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Nanometre-thin indium tin oxide for advanced high-performance electronics

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Although indium tin oxide (ITO) is widely used in optoelectronics due to its high optical transmittance and electrical conductivity, its degenerate doping limits exploitation as a semiconduction material. In this work, we created short-channel active transistors based on an ultra-thin (down to 4 nm) ITO channel and a high-quality, lanthanum-doped hafnium oxide dielectric of equivalent oxide thickness of 0.8 nm, with performance comparative to that of existing metal oxides and emerging two-dimensional materials. Short-channel immunity, with a subthreshold slope of 66 mV per decade, off-state current <100 fA μm^{-1} and on/off ratio up to 5.5 × 10^9, was measured for a 40-nm transistor. Logic inverters working in the subthreshold regime exhibit a high gain of 178 at a low-supply voltage of 0.5 V. Moreover, radiofrequency transistors, with as-measured cut-off frequency f_T and maximum oscillation frequency f_{max} both >10 GHz, have been demonstrated. The unique wide bandgap and low dielectric constant of ITO provide prospects for future scaling below the 5-nm regime for advanced low-power electronics.

Despite recent progress in material synthesis and device optimizations, the performance and application gap between thin-film transistors (TFT) and high-performance transistors has persisted with no viable solution in prospect[1]. Decades of effort have been spent on investigation of novel channel materials, mainly emerging nano-materials including carbon nanotubes and two-dimensional (2D) materials[2]. Although the low-dimensional nature of these materials offers the intrinsic advantage of electronic control in deeply scaled nano-transistors, very few of these materials have provided a competitive edge regarding either existing TFT technology[1–44] or advanced high-performance, silicon (Si)-based transistors[45–50]. The greatest challenges are large-area material synthesis and device performance, as well as other key issues such as thermal budget and process compatibility with the existing planar platform. Indium tin oxide (ITO) is a highly conductive, tin-doped semiconductor with a wide bandgap of around 3.5 electronvolts (eV) and mobility of around 30 cm^2 V^{-1}s^{-1} (refs. [8–12]). ITO is currently rarely used as an active channel material due to its unsatisfactory switching performance, with only a small number of micrometre-long devices for TFT drivers having been demonstrated (see details in Supplementary Table 2). However, as a transparent conducting oxide, it is the material most widely used in coatings, solar cells and, most importantly, the display industry—from modern television sets and computers to mobile phones—and is, in principle, virtually ubiquitous in screens used for information and entertainment via visual perception in everyday life[1,5–12]. Such a well-developed material with industry-wide availability has very intriguing electronic properties that are desirable as an active channel material, in both TFT and high-performance electronic transistors[1–7].

The previous low resistivity of ITO (around 10^{-4} Ω cm) originated from high-electron doping by oxygen vacancy and substitutional tin dopants, which fixes the Fermi level to the conduction band edge and results in metallic behaviour[8–12]. Reduction in thickness has been shown to be effective in bandgap increase and free carrier depletion in other material systems, including recently developed 2D materials[1,2]. More importantly, the ultra-thin-body silicon-on-insulator (SOI) has demonstrated success in the field of advanced low-power silicon technology, as fully depleted SOI[45–49], on a par with the fin field-effect transistor (FinFET) technology[50], with both showing substantially improved short-channel immunity in ultimately scaled devices. As the quest for low consumption and standby power in consumer electronics intensifies, transistors with ultra-low off-state current that maintain high on-state current, and which guarantee low static power dissipation and high driving speed, are much sought after[45,46]. However, the off-state current of ultimate short-channel silicon transistors—for example, 22-nm FinFET low-power transistors[50]—is limited to around 1 pA μm^{-1}, mainly ascribed to direct tunnelling and thermionic currents, which are determined by a silicon bandgap of 1.12 eV and material properties such as natural length, λ (refs. [48,49]). In this work, by adopting the properties of ultra-thin-body silicon and 2D materials, together with the interface and intrinsic material engineering, fully depleted ultra-thin-body ITO was developed showing excellent electronic properties that are desirable in ultra-low-power applications. Using the physical vapour deposition radiofrequency (RF) sputtering method with optimized oxygen partial pressure, oxygen vacancy can be largely eliminated and effective Fermi-level movement obtained through electrostatic control. Systematic investigation of channel thickness and gate dielectrics weas carried out with channel length (L_{ch}) scaling down to 40 nm, the material exhibiting excellent off-state properties as well as on-state performance. Furthermore, practical electronic components such as logic inverters operating in the subthreshold region with an ultra-high gain, as well as high-performance radiofrequency transistors beyond 10 GHz, were demonstrated. With advantages including wide bandgap, amorphous channels, good mobility and large-scale availability, the ultra-thin-body ITO has great future potential in electronics.

ITO film was formed by standard radiofrequency sputtering using a commercially available ITO target at 200 °C in an oxygen-rich environment to decrease the oxygen vacancy, and an optimized vapour pressure ratio of 1/9 for oxygen/argon gas was used (see Supplementary Sections 1.1 and 3.1 for details). The thinnest film

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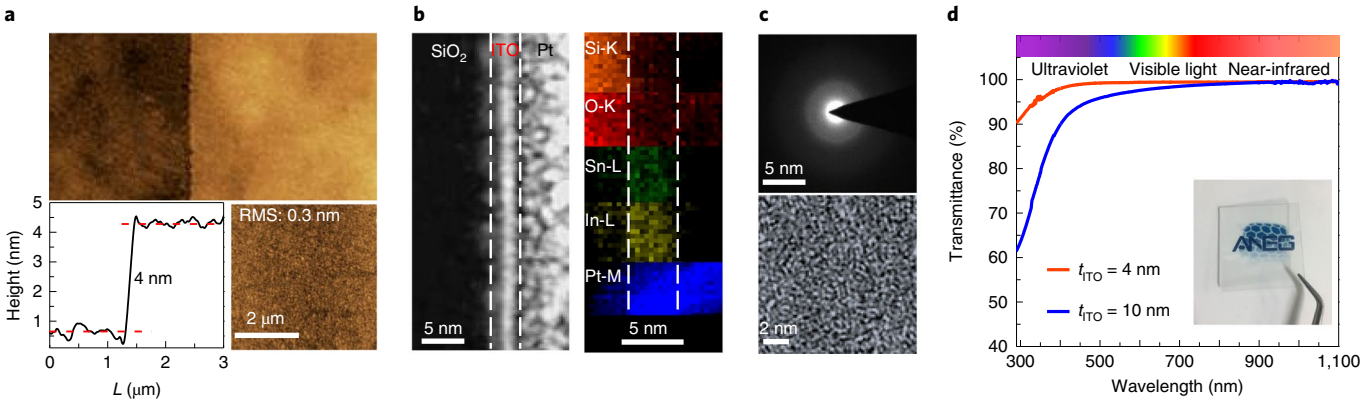

Fig. 1 | Material characterization of thin ITO film. a, Atomic force microscopy images of ITO film. The surface root mean square roughness is 0.3 nm. **b**, Cross-section TEM analysis and corresponding high-resolution EDX mapping of elements silicon (Si), oxgen (O), tin (Sn), indium (In) and platinum (Pt). K, L, M represents different atomic energy levels. The region defined by the dashed lines indicates the ITO layer. Scale bars, 5 nm. **c**, Selected area electron diffraction pattern of amorphous ITO film with incidence angle in the perpendicular direction (upper) and high-magnification plane TEM image (lower). **d**, Optical transmission spectrum of ITO films of varying thickness. Inset: optical image of 4-nm ITO film on a glass substrate.

applied in this work was 4 nm, with a root mean square roughness of 0.3 nm, as shown in Fig. 1a. Such atomically smooth topography is crucial for a high-quality interface, to minimize surface roughness scattering. This ultra-thin channel was further confirmed by cross-section, high-magnification transmission electron microscopy (TEM) images as shown in Fig. 1b. The corresponding high-resolution, energy-dispersive X-ray spectroscopy (EDX) shown in the right-hand panel of Fig. 1b was utilized to confirm the material composition of the same region in the TEM image. The selected area electron diffraction pattern was used to confirm the amorphous state of the resulting 4-nm ITO film, as shown in the upper panel in Fig. 1c. This amorphous state should provide better uniformity and temperature stability compared to the polycrystalline state[6]. As shown in Fig. 1d, the light transmittance for the 4-nm film is high throughout the infrared and visible spectra, with high transparency of 90% even at the ultraviolet region around 300 nm. The 4-nm ITO deposited on the glass is visually fully transparent, as shown in the inset of Fig. 1d. We extracted a bandgap of 3.7 eV for 4-nm ITO using Tauc plots, and the dependence of bandgap on film thickness is summarized in Supplementary Section 1.2.

Figure 2a–c shows channel length ranging from 30 μm to 40 nm with the systematic studied on device structures of ITO transistors by varying the gate dielectric material, channel thickness ($t_{channel}$) and dielectric thickness (t_{oxide}). Note that the thermal budget of the device fabrication process was 300 °C, which is the depositing temperature of the dielectric, and there is no annealing process after film deposition. Figure 2d–f shows the corresponding I_{ds}–V_{gs} transfer characteristics, where I_{ds} is the drain current and V_{gs} is the gate to source voltage. For the long-channel device of 30 μm shown in Fig. 2a,d, both transistors with a $t_{channel}$ of 10 nm can be fully turned off, except that the device with a 20-nm, high dielectric constant (high-k), La-doped hafnium oxide (HfLaO) dielectric can operate in the region that is normally off, with much better subthreshold slope (SS) in the saturation region and with a drain voltage of 2 V, suggesting that free carriers in the channel are fully depleted with better electrostatic control provided by the combination of thin channel and thin equivalent oxide thickness (EOT) of 3 nm. HfLaO shows not only a higher dielectric constant, but also enhanced ability, to reduce gate leakage current (see Supplementary Sections 1.4 and 3.2 for details). When the length of the device channel was reduced from 30 to 3 μm with the same 20-nm HfLaO dielectric shown in Fig. 2e, the threshold voltage shifted negatively by 5 V, meaning that the channel could not be turned off completely at zero gate bias at a drain voltage of 2 V due to the lateral electric field effect. Further reduction in channel thickness, from 10 to 4 nm, effectively moved the threshold voltage positively by >3 V and restored the operation that is normally off (Fig. 2e), which can be ascribed to the better off-state and short-channel immunity of the fully depleted channel of 4 nm[2].

Despite the ultra-thin 4-nm channel used for the ITO transistor, carrier transport is subjected to minimal effect from energy quantization and surface scattering (see Supplementary Sections 3.4 and 3.5 for details). Figure 2f shows the transfer characteristics of a short-channel device of 40 nm with oxide thicknesses of 20 and 5 nm at $t_{channel}$ = 4 nm, at drain bias V_{ds} of 0.05 and 2 V, respectively. The 40-nm-long device exhibits a maximum and minimum on-current ratio, $I_{on}/I_{off} > 10^9$ at V_{ds} = 2 V, and SS < 70 mV per decade for three orders, much better than corresponding values for the thicker oxide device owing to the superior electrostatic control and reduced short-channel-effect (SCE) provided by the thinner EOT. In general, SCE begins to affect device behaviour significantly once the channel length is reduced to around threefold its natural length[1,48,49]. Natural length is defined as $\lambda = \sqrt{\frac{\varepsilon_s}{\varepsilon_{SiO_2}} \mathrm{EOT} \times t_{channel}}$, where ε is the permittivity of the semiconductor material and t_s is channel thickness. It can be seen that ultra-thin EOT, t_s and lower semiconductor permittivity can reduce natural length. ITO exhibits a lower permittivity of around 4 compared with Si (~11.7)[3,9] and, in combination with 4-nm $t_{channel}$ and 0.8-nm EOT, a natural length of around 1.8 nm is sufficiently small and results in negligible SCE in a 40-nm device. In view of the importance of λ for SCE, we compare its dependence on $t_{channel}$ for the silicon and ITO channels with varying gate dielectrics in the calculations shown in Fig. 2g. Among the three structures, we can see that ITO/5-nm HfLaO has the lowest λ (<2 nm at $t_{channel}$ = 4 nm), indicating excellent short-channel immunity for very highly scaled transistors. In the low-power operation, a high on/off ratio and low SS help in scaling down supply voltage for low-power operations[2]. These two advantages optimized by $t_{channel}$, with EOT = 3 nm and t_{oxide} with $t_{channel}$ = 4 nm, are summarized in Fig. 2h, with SS of 66 mV per decade and on/off ratio up to 5.5×10^9, while the leakage current in the off-state is <100 fA μm^{-1}, as shown in Fig. 2f. Both exceed the SS of 75 mV per decade and on/off ratio <10^8 ($I_{on\text{-}max}/I_{min}$) for SOI[45,46].

Figure 3a shows a comparison of the critical parameter drain-induced barrier lowering (DIBL) of ITO and other materials as a function of channel length. Transistors based on ITO show much lower DIBL, of only 60%, of the ultra-thin-body SOI devices at a similar channel thickness of 3.8 nm (ref. [47]), which is much lower

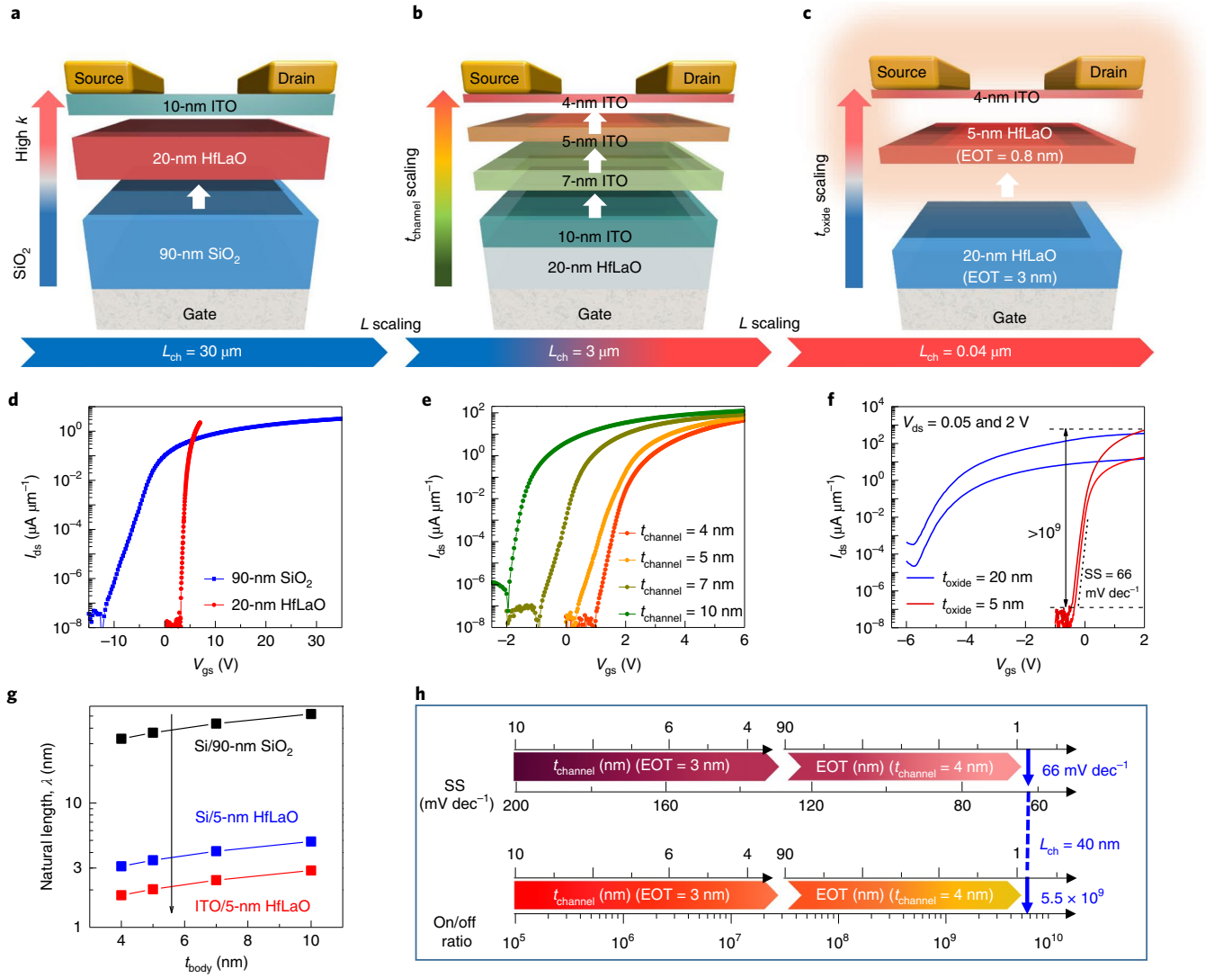

Fig. 2 | Device structure and direct current electrical characteristics. a–c, Schematics of ITO transistor structures with channel length 30 μm, channel thickness 10 nm and dielectric 20-nm HfLaO or 90-nm SiO_2 (**a**); with channel length 3 μm, channel thickness 4, 5, 7 and 10 nm and dielectric 20-nm HfLaO (**b**); and with channel length 0.04 μm, channel thickness 4 nm and dielectric 5- or 20-nm HfLaO (**c**). **d–f**, Transfer characteristics (I_{ds}–V_{gs}) corresponding to **a** (**d**), **b** (**e**) and **c** (**f**). **g**, Natural length (λ) as a function of $t_{channel}$ for silicon and ITO with different dielectrics. **h**, SS and on/off ratio summary, as $t_{channel}$ with EOT = 3 nm and EOT with $t_{channel}$ = 4 nm; with L_{ch} = 40 nm.

than that of the latest 2D materials[18–22]. To better understand the advantages of the ultra-thin-body ITO transistor in the off-state region, we compare the energy band diagram between Si and ITO in Fig. 3b. At $V_{gs} < V_{FB}$, where V_{FB} is the flatband voltage, there are two main contributors to the off state[51]: thermionic leakage current J_T ($J_T \propto \exp(-\Phi)$) and direct tunnelling current J_{DT} ($J_{DT} \propto \exp(-\Phi \times W)$), where Φ is the surface potential and W is the minimum length of surface potential without drain voltage influence, which is directly proportional to λ[48,49]. These two equations indicate that J_T and J_{DT} are both in an exponential relationship with Φ, while J_{DT} additionally will be influenced by W, which is essentially the tunnel barrier width. In addition to the lower value of λ as discussed above, ITO has much greater inbuilt potential than Si because of the wide bandgap, resulting in significantly reduced $I_{leakage}$ and DIBL, as shown in the right-hand panel of Fig. 3b.

Figure 3c–e shows output characteristics I_{ds}–V_{ds} curves for ITO transistors with λ = 5.5 nm ($t_{channel}$ = 10 nm, t_{oxide} = 20 nm), λ = 3.5 nm ($t_{channel}$ = 4 nm, t_{oxide} = 20 nm) and λ = 1.8 nm ($t_{channel}$ = 4 nm, t_{oxide} = 5 nm), respectively (see Supplementary Section 3.3 for details). We obtained the maximum output current, I_{ds} of 520 μA μm^{-1} in the device for λ = 1.8 nm at V_{ds} = 2 V for the 40-nm-long transistor. The output current was higher for the device with λ = 3.5 nm with 100-nm channel length of around 850 μA μm^{-1}, which can be attributed to the higher electron doping from a much larger gate overdrive. When one factor is the difference in EOT, together with the inversion layer thickness of around 1 nm, the drain current of this transistor is around 200 μA μm^{-1} at gate overdrive similar to the thinner EOT device, which is consistent with other 100-nm channel devices. Notably, the output current exceeded 1.15 mA μm^{-1} for the device with λ = 5.5 nm and 200-nm channel length, which can be attributed to the thicker channel with higher carrier density and better access resistance. Figure 3f shows the benchmark of $I_{on\text{-}max}$ as a function of on/off ratio in comparison with other technology, including both 2D materials and metal oxide transistors (see Supplementary Table 3 for details); all the data presented here relate to short-channel devices of L_{ch} <200 nm, for technological relevance. Note here that on/off ratios were extracted as the maximum on-current at highest gate overdrive and minimal off-current from the transfer characteristics

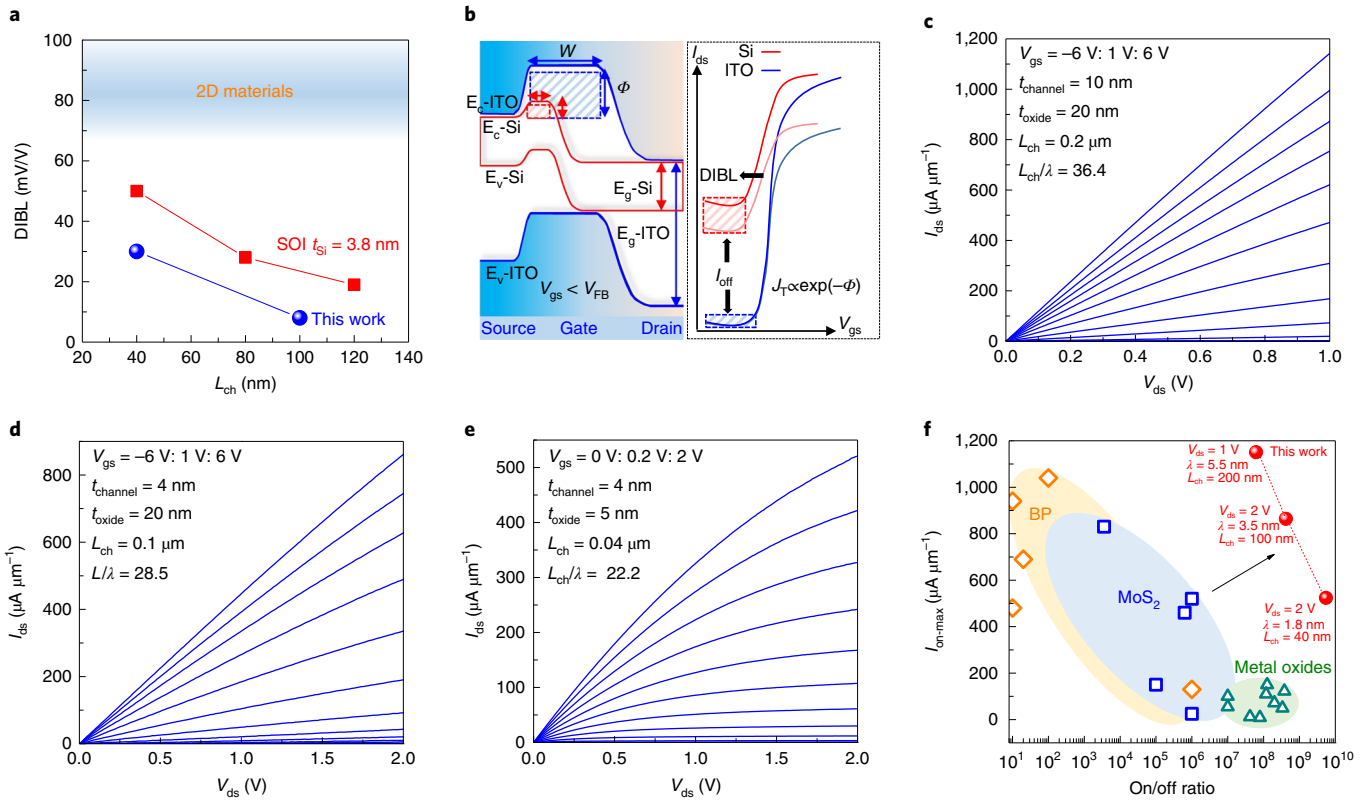

Fig. 3 | Off-state and on-state performance of ITO transistors. a, DIBL versus channel length for devices studied in this work and an ultra-thin-body SOI field-effect transistor (FET). **b**, The energy band diagram illustrates ITO transistors and Si FET operating in the off state ($V_{gs} < V_{FB}$) (left), in which W and Φ represent the width and height of the potential barrier, respectively. E_c, E_v and E_g represent the conduction-band minimum, valence-band maximum and bandgap, respectively. Transfer characteristics comparison I_{ds}–V_{gs} of ITO transistors (blue line) and Si (red line) and FET at varying V_{ds} (right). Off-state current (I_{off}) is shown in the inset box. **c**, Output characteristics I_{ds}–V_{ds} for 200-nm-long transistor with $t_{channel}$ = 10 nm and t_{oxide} = 20 nm, with V_{gs} ranging from –6 to 6 V in steps of 1 V. **d**, Output characteristics I_{ds}–V_{ds} for 100-nm-long transistor with $t_{channel}$ = 4 nm and t_{oxide} = 20 nm, with V_{gs} ranging from –6 to 6 V in steps of 1 V. **e**, Output characteristics I_{ds}–V_{ds} for 40-nm-long transistor with $t_{channel}$ = 4 nm and t_{oxide} = 5 nm, with V_{gs} ranging from 0 to 2 V in steps of 0.2 V. **f**, Benchmark of $I_{on\text{-}max}$ versus on/off ratio for <200-nm-long ITO, black phosphorus (BP), MoS_2 and metal oxide transistors. The extracted data are listed in Supplementary Table 3.

for each device. Despite the fact that these devices are not necessarily biased at the same conditions for different technologies, with maximum V_{ds} varying from ~1–4 V, this comparison still demonstrates the competitiveness and performance potential of the channel material. The maximum on-current of the ITO transistors is more than fivefold higher than that of the best metal oxide transistors. Also, it can be seen that the ITO transistor achieved concomitantly both the highest I_{on} and on/off ratio. For transistors with output current >1 mA μm^{-1} based on black phosphorus, the on/off ratio of the ITO transistor is around six orders of magnitude higher with even slightly higher on-current. Here we note that a reduction in operation bias can be achieved by further optimization of oxide thickness, threshold voltage, contact resistance and channel length.

It is important to note the presence of an extremely small DIBL region in an extended SS region expanding for more than three decades, indicating that the output resistance was sufficiently high to obtain a high intrinsic gain[25]. Figure 4a shows the transfer characteristics for a 0.5-μm-long transistor in the subthreshold region with the same channel thickness of 4 nm and EOT of 0.8 nm. It can be seen that the DIBL of this device approaches zero, and therefore the output resistance of $1/g_d$ where g_d is the output conductance, is above 10 MΩ, as shown in Fig. 4b. We calculate the g_m, which is the transconductance, and $1/g_d$ as a function of V_{gs} in Fig. 4c; the intrinsic gain, defined as $A_i = g_m/g_d$, is as high as 1,000 biased at 0.2–0.6 V, as shown in Fig. 4d, which is much higher than that for other metal oxide transistors or 2D materials and almost two orders of magnitude higher than that for Si metal–oxide–semiconductor field-effect transistors. Based on this, we demonstrate an enhancement–depletion mode inverter using ITO transistors, where the structure is shown in the inset of Fig. 4e. This inverter exhibits full swing output at a supply voltage V_{dd} = 0.5 V and high transfer gain of 178, with the highest gain of 467 being obtained at V_{dd} = 2.5 V (Supplementary Section 4.1). In comparison with other devices from the literature, shown in Fig. 4f, the gain is twofold at the same supply voltage of 2 V and >100-fold at 0.5 V, much higher than that for previously documented metal oxides or 2D materials (see Supplementary Table 4 for details). This high gain is enabled by the negligible DIBL in the broad, steep SS region, which is essential for low-power operation while maintaining high gain, and can help boost performance in many portable electronic devices.

To further evaluate high performance in the saturation region, we fabricated high-frequency transistors based on these ITO transistors and conducted an RF measurement to extract high-frequency scattering parameters (S) illustrated in Fig. 5a. Our measurements were performed using a two-port configuration, the details of which can be found in Supplementary Section 5.1. The channel length of the RF transistors was designed as 40, 100 and 200 nm and confirmed by scanning electron microscopy images (Fig. 5b), with the same channel body thickness of 4 nm and EOT of 0.8 nm. The transconductance, g_m, at the saturation region reached 536 μS μm^{-1}

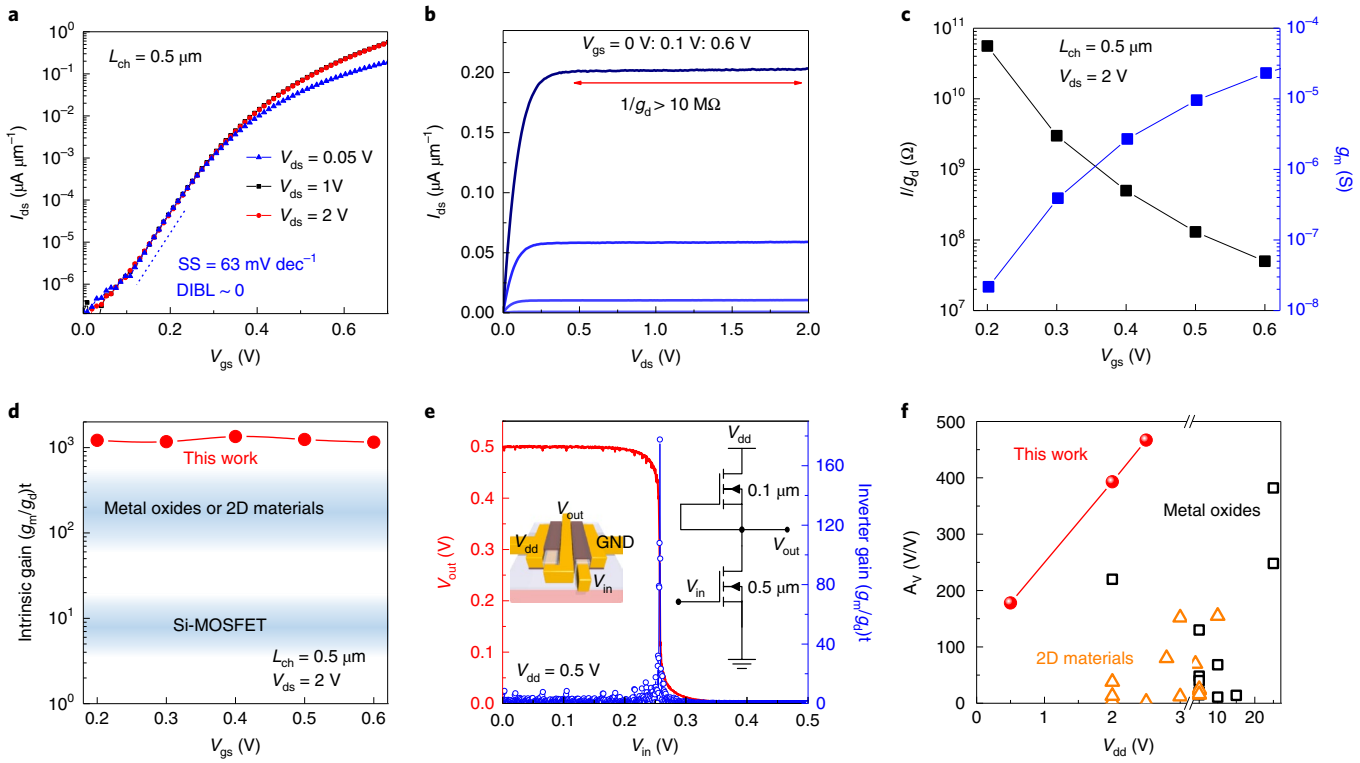

Fig. 4 | Logic inverters based on ITO transistors with high gain. a, Transfer characteristics of ITO transistors of channel length 0.5 μm at V_{ds} = 2, 1 and 0.05 V. **b**, Output characteristics of the same transistor, with V_{gs} = 0–0.6 V in steps of 0.1 V. **c**, Extracted values of $1/g_d$ (black squares) and g_m (blue squares) as a function of V_{gs} at V_{ds} = 2 V. **d**, Measured intrinsic gain, g_m/g_d, as a function of V_{gs}. **e**, Output voltage and inverter gain for the logic inverter as a function of input voltage at 0.5 V. Inset: schematic view of the enhancement-depletion mode inverter. **f**, Benchmark of inverter gain as a function of V_{dd} for inverters based on metal oxides, 2D materials and ITO transistors in this work. The extracted data are listed in Supplementary Table 4.

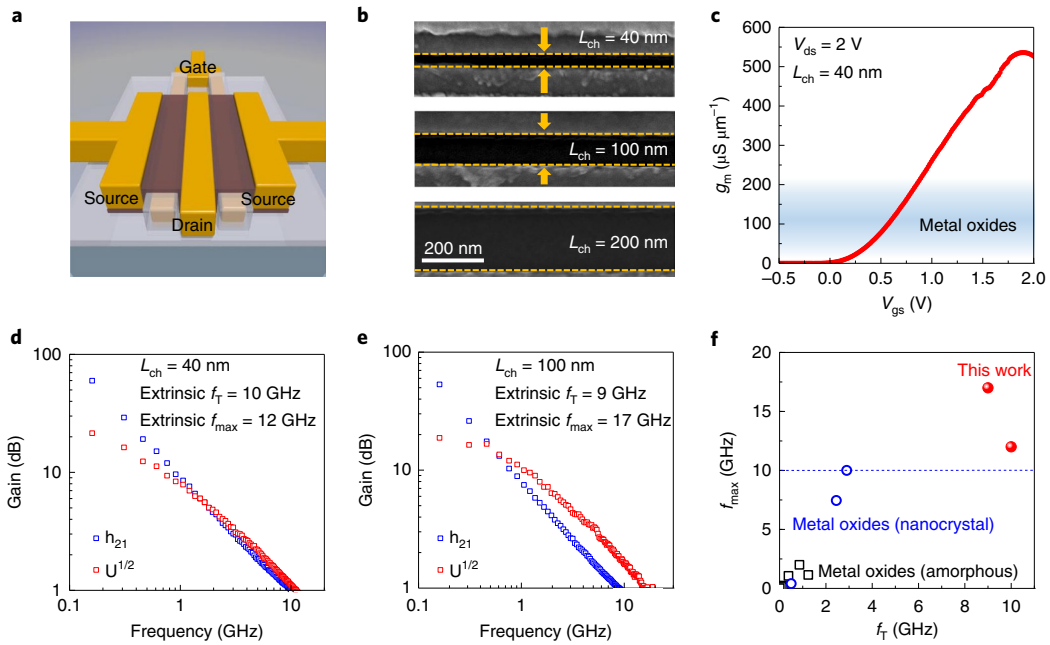

Fig. 5 | High performance of RF transistors based on ITO. a, Schematic view of the RF transistor structure. **b**, Scanning electron microscopy image of channel lengths 40, 100 and 200 nm. **c**, Transconductance (g_m) as a function of V_{gs}, L_{ch} = 40 nm. **d**, Low-signal current gain, h_{21} (blue squares), and Mason's unilateral gain, $U^{1/2}$ (red squares), versus frequency for the 40-nm-long device with extrinsic cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) of 10 and 12 GHz, respectively. **e**, Low-signal current gain (h_{21}) (blue squares) and $U^{1/2}$ (red squares) versus frequency for the 100-nm-long device with f_T and f_{max} of 9 and 17 GHz, respectively. **f**, Benchmark of f_T and f_{max} with other metal oxide transistors. The extracted data are listed in Supplementary Table 7.

at $V_{ds} = V_{gs} = 2$ V for the 40-nm transistor, as shown in Fig. 5c, much higher than any that of other metal oxide transistors[13–16,33–39]. The cut-off frequency, f_T, and maximum oscillation frequency, f_{max}, are key to evaluation of RF performance[4]. As-measured extrinsic $f_T = 10$ GHz and $f_{max} = 12$ GHz were obtained for the 40-nm-long device, as shown in Fig. 5d, while $f_T = 9$ GHz and $f_{max} = 17$ GHz were obtained for the 100-nm-long device, as shown in Fig. 5e. We also demonstrated that the 4-nm ITO transistor possesses better RF performance compared to those with a thicker channel (Supplementary Section 5.2). Because of low effective velocity (~3×10^5 cm s^{-1}) and poor saturation characteristics in the short channel for amorphous-state devices[33–36], the levels of f_T and f_{max} of these transistors were found to be <5 GHz. The performance benchmark of the these critical RF parameters is summarized in Fig. 5f for metal oxide-based RF transistors whereas those analysed in this work exhibited excellent performance, with extrinsic f_T and f_{max} both >10 GHz (see Supplementary Table 7 for details). Extrinsic f_T was also higher than that of 2D semiconductors, including recent work on chemical vapour deposition bi-layer molybdenum disulfide (MoS_2) (refs. [40–44]). Further improvement was achieved using optimized device structures, such as a self-aligned gate and doped source/drain area, to minimize parasitic capacitance and access resistance, and intrinsic high-frequency performance was significantly improved, as seen in the advanced design system simulations shown in Supplementary Section 5.3.

In summary, ultra-thin-body ITO transistors with ultra-thin EOT structure were used for low-power, high-performance, short-channel logic and RF transistors. The lowest off-current and highest on/off ratio were achieved for the device with 40-nm channel length and excellent short-channel immunity. A logic inverter with high gain at low-supply power of 0.5 V was demonstrated. Furthermore, high-performance RF transistors, with f_T and f_{max} both >10 GHz, were also demonstrated. This work introduces further possibilities for the next generation of low-cost, low-power electronics.

Online content

Any methods, additional references, Nature Research reporting summaries, source data, statements of code and data availability and associated accession codes are available at https://doi.org/10.1038/s41563-019-0455-8.

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Author contributions

Y.W. proposed and supervised the project. S.L. and M.W. fabricated the devices. S.L. performed morphology and electrical measurements. S.L., M.T., Q.G. and T.L. performed the RF characterizations. S.L. and Q.H. discussed the device designs. S.L., X.L. and Y.W. analysed the data. S.L. and Y.W. co-wrote the paper. All authors contributed to discussions on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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Methods

(1) Material characterizations: atomic force microscopy was performed using a SPM9700 (Shimadzu, Inc.) in tapping mode. High-resolution TEM imaging and high-resolution EDX were performed using a Tecnai G2 F30 (FEI, Inc.) operated at 300 kV. Optical transmission spectroscopy was performed with a Lambda 35 (PerkinElmer, Inc.) with spectrum ranging from 300 to 1,100 nm. Further details can be found in Supplementary Section 1.

(2) Fabrication process: ITO transistors fabricated in this work are based on the staggered bottom gate structure. The substrate was high-resistance (>10,000 Ω cm) silicon coupled with 90-nm SiO_2. The gate was first patterned on the substrate using electron-beam lithography, following by a metallization process (nickel (20 nm)/gold (80 nm)/nickel (3 nm)). HfLaO was deposited by atomic layer deposition as the gate oxide. The gate window was patterned and etched by inductively coupled plasma. ITO film was then deposited by sputtering from a sputter target of In_2O_3/SnO_2 (90/10 wt%). To ensure uniformity, we deposited the film at a rate of 1.3 nm min^{-1} by controlling the RF power and chamber pressure. Finally, we deposited source/drain contact with nickel (20 nm)/gold (80 nm). Further details can be found in Supplementary Section 2.

(3) Electrical characterization: The *I*–*V* and RF characteristics were measured under vacuum (~10^{-4} Torr) in a Lakeshore vacuum probe station using the Agilent B1500A Semiconductor Device Analyzer and the PNA Network Analyzer. Further details can be found in Supplementary Sections 3–5.

Data availability

The data supporting the figures within this paper are available from the corresponding author upon reasonable request.