MATERIALS SCIENCE

High-speed black phosphorus field-effect transistors approaching ballistic limit

Xuefei Li[1]*, Zhuoqing Yu[2]*, Xiong Xiong[1], Tiaoyang Li[1], Tingting Gao[1], Runsheng Wang[2], Ru Huang[2], Yanqing Wu[1,2†]

As a strong candidate for future electronics, atomically thin black phosphorus (BP) has attracted great attention in recent years because of its tunable bandgap and high carrier mobility. Here, we show that the transport properties of BP device under high electric field can be improved greatly by the interface engineering of high-quality HfLaO dielectrics and transport orientation. By designing the device channels along the lower effective mass armchair direction, a record-high drive current up to 1.2 mA/μm at 300 K and 1.6 mA/μm at 20 K can be achieved in a 100-nm back-gated BP transistor, surpassing any two-dimensional semiconductor transistors reported to date. The highest hole saturation velocity of 1.5 × 10^7 cm/s is also achieved at room temperature. Ballistic transport shows a record-high 36 and 79% ballistic efficiency at room temperature and 20 K, respectively, which is also further verified by theoretical simulations.

INTRODUCTION

Two-dimensional (2D) semiconductors are gaining considerable attention far beyond silicon electronics because of their ultrathin bodies and high carrier mobility (*1*, *2*). Recently, the discovery of the excellent electronic performance of black phosphorus (BP) transistors has stimulated widespread research interest. Experiments have shown that the BP field-effect transistors (FETs) exhibit ambipolar behavior with on/off ratio up to 10^6 and mobility up to ~1000 $cm^2/V·s$ (*3*). Meanwhile, the direct bandgap of BP varies from 0.3 eV (bulk) to 2.0 eV (monolayer), making it suitable for applications in optoelectronics, especially in the infrared regime (*4*). Since 2014, many efforts have been made on the 2D BP films with regard to logic and optoelectronic applications (*5*, *6*); high-performance BP devices under high electric field are still lacking. One issue is the formation of Schottky barriers at the interface between BP and metal contacts, resulting in relatively large contact resistance (R_c) that severely limits the device performance especially in short-channel regime (*7*, *8*). Most previous works focus on high work function metal or chemical doping to enhance the hole injection and decrease the R_c (*5*, *9*). However, typical contact resistance values resulting from these methods are still around 1 kilohm·μm, and the drive current of these devices is limited in the range of 0.2 to 0.7 mA/μm. As a result, effective doping approach for high-performance BP transistors is still lacking. In addition, it has been well known that the impurities and the dielectric environment play important roles in the electrical and optical properties of the sensitive BP materials (*10*). So far, most studies focus on BP devices with thick thermally oxidized SiO_2 as back-gated dielectrics, which typically yield unsatisfactory electronic properties (*3*–*5*, *9*). Therefore, the integration of high-quality dielectrics with BP is an important scientific and technological challenge. Another unique property of BP is its anisotropic properties due to the highly asymmetric effective mass, which enables the use of the lower effective carrier mass transport along the armchair direction for better performance transistors (*4*). Moreover, saturation velocity plays a substantial role in determining device performance especially in short-channel transistors, and hole saturation velocity in conventional semiconductors and 2D transition metal dichalcogenides is typically much lower than that of electrons. High hole saturation velocity in BP 2D semiconductors is vital for realizing high-performance optoelectronics and electronics (*11*). However, very few studies of saturation velocity in short-channel BP FETs have been reported to date despite the importance in fundamental and practical application.

In this work, we introduce an ultrathin high-*k* HfLaO as the back gate dielectric to increase the electrostatic doping and improve the interface quality. The equivalent oxide thickness of the HfLaO dielectric in this work is around 2.7 nm. The application of −4 V back gate (V_{bg}) voltage induces a much higher carrier density of 2.1 × 10^{13} cm^{-2} than those using the typical SiO_2, owing to the combination of high-*k* property and excellent dielectric breakdown property. The high carrier density results in an increase of electrostatic doping of BP underneath the metal contact with a lower Schottky barrier, which facilitates the hole injections from the source metal into the channel that results in a reduced R_c. The minimal R_c of 0.7 kilohm·μm and the maximum drain current of 1.2 mA/μm for the 100-nm channel length BP device are obtained at room temperature. Furthermore, the drain current increases to around 1.6 mA/μm at 20 K when ballistic transport is effectively realized. In addition, we extract a saturation velocity of 1.5 × 10^7 cm/s at room temperature, which outperforms silicon and other layered 2D semiconductors and reaches the highest value for hole saturation velocity.

RESULTS AND DISCUSSION

Device fabrication

We mechanically exfoliated layered BP flakes from bulk crystal (smart elements) and then transferred them onto a p^{++} Si substrate covered with HfLaO dielectric layer. The dielectric constant of the HfLaO film is 26 (figs. S1 to S3). The schematic view of the dual-gated devices in this work is shown in Fig. 1A. The channel region is defined by electron beam lithography and followed by a 20-nm Ni/60-nm Au metal stack by electron beam evaporation as source and drain electrodes. The BP flakes were identified by a combination of optical microscopy and atomic force microscopy (AFM) with typical thickness around 12.5 nm, as shown in Fig. 1B. Raman spectra on the 12.5-nm-thick BP flake

[1]Wuhan National High Magnetic Field Center and School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan 430074, China. [2]Institute of Microelectronics and Key Laboratory of Microelectronic Devices and Circuits (MOE), Peking University, Beijing 100871, China.
*These authors contributed equally to this work.
†Corresponding author. Email: yqwu@pku.edu.cn

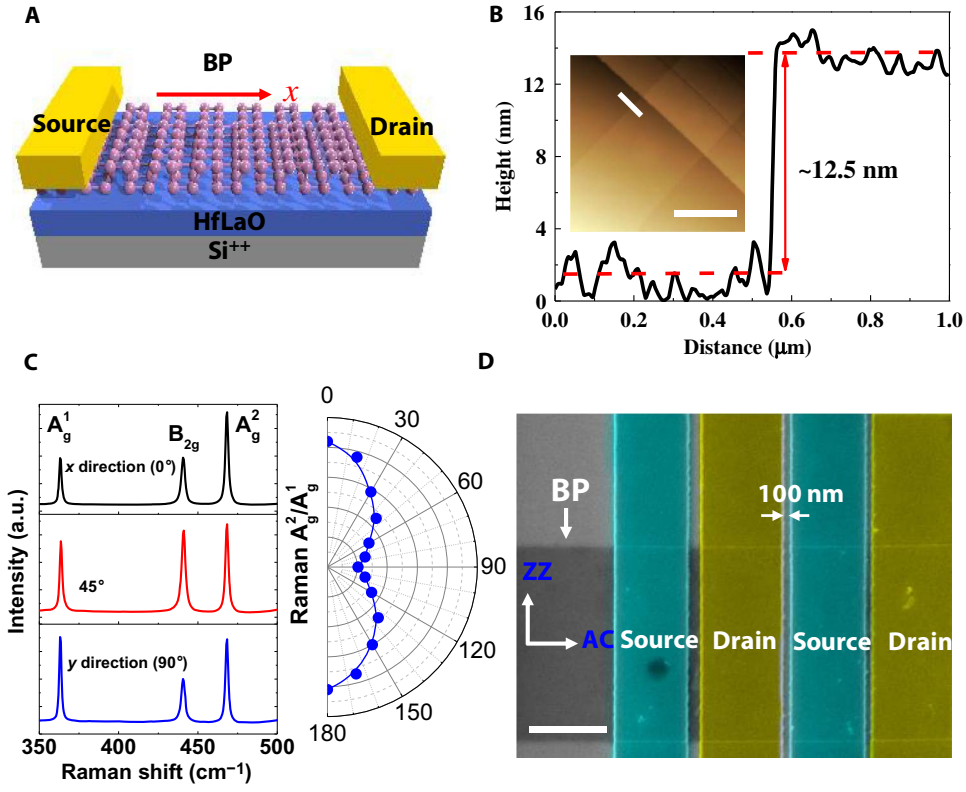

Fig. 1. Characterization of the device structure. (**A**) Schematic of a back-gated BP on an HfLaO substrate with top Ni/Au source and drain electrodes. (**B**) BP flake with a measured thickness of 12.5 nm by AFM. Inset of (B), AFM image of the few-layer BP devices. Scale bar, 2 μm. (**C**) Polarization-resolved Raman spectrum of the BP flake. The left image shows three spectra obtained from an individual flake in different orientations. The right image shows the orientation-dependent A_g^2/A_g^1 peak intensities. (**D**) Representative false-colored SEM image of the BP transistors. AC and ZZ stand for the armchair and zigzag directions, respectively. Scale bar, 1 μm. a.u., arbitrary units.

with the excitation laser polarized along three different directions are shown in the left panel of Fig. 1C. The three characteristic Raman modes, A_g^1, B_{2g}, and A_g^2, can be observed, corresponding to the out-of-plane vibration along the *z* axis (~361 cm^{-1}), in-plane vibration along the *y* axis (zigzag) (~438 cm^{-1}), and armchair (~466 cm^{-1}) directions along the *x* axis, respectively (*4*, *5*). As shown in the A_g^2/A_g^1 intensity ratio in 180° rotation of the sample in the right panel of Fig. 1C, it is clear that the intensity ratio reaches the maximum and minimum values when the laser polarization is parallel to the *x* (armchair) and *y* (zigzag) directions, respectively, consistent with the anisotropy of BP (*4*). Figure 1D shows a typical scanning electron microscopy (SEM) image of the fabricated BP transistors, with a channel length of 100 nm in this work. To achieve the best performance, we aligned the metal contact to the zigzag crystal direction of the BP flake to achieve the electronic transport in the channel along the armchair direction (*4*).

Temperature-dependent transport properties of BP transistors

Figure 2A shows the well-behaved output characteristics of BP FETs with the 100-nm channel length at room temperature. A maximum drain current (I_{dmax}) of 1.2 mA/μm is realized at V_d = −2.5 V and V_{bg} = −4 V, which is the highest on-current density reported for BP transistors at room temperature to date, to the best of our knowledge (*12*, *13*). As shown in Fig. 2B, a record-high I_{dmax} of 1.6 mA/μm is obtained at V_d = −2.5 V and V_{bg} = −5 V at 20 K, which is the highest current reported thus far for all 2D semiconductor materials (*12*, *13*). The corresponding transfer characteristics for the same BP device are shown in fig. S4 (A and B). Contact resistance R_c is extracted using the transfer length method, and the result is shown in fig. S5A. In addition, the Schottky barrier height of metal-BP contacts shows a strong back gate dependence, and a very small contact resistance can be achieved at higher doping densities from the back gate voltage (fig. S5, A and B). The details of the carrier injection mechanism are shown in fig. S5 (C to E). The gate voltage of the minimum drain current (V_{min}) for BP on the HfLaO dielectric substrate remains the same as the temperature decreases from 300 to 20 K, as shown in Fig. 2C, suggesting minimal interface trap charges between the BP flake and the HfLaO dielectric. This can be further confirmed by plotting the difference of threshold voltage during double sweeps at different temperatures, as shown in Fig. 2D, showing that the gate voltage hysteresis is independent of temperature. The weak temperature dependence of the V_{min} and hysteresis indicates reduced interface trap densities and charge inhomogeneities (*14*, *15*).

Saturation velocity in BP FETs

We assume that the electric field and charge are uniform along the channel and ignore the drain-induced barrier-lowering effect. In this case, the carrier velocity υ_d across the channel can be derived by

$$\upsilon_d = \frac{I_d}{W|Q|} = \frac{I_d}{WC_g|V_{gs} - V_t - V'_d/2|} \quad (1)$$

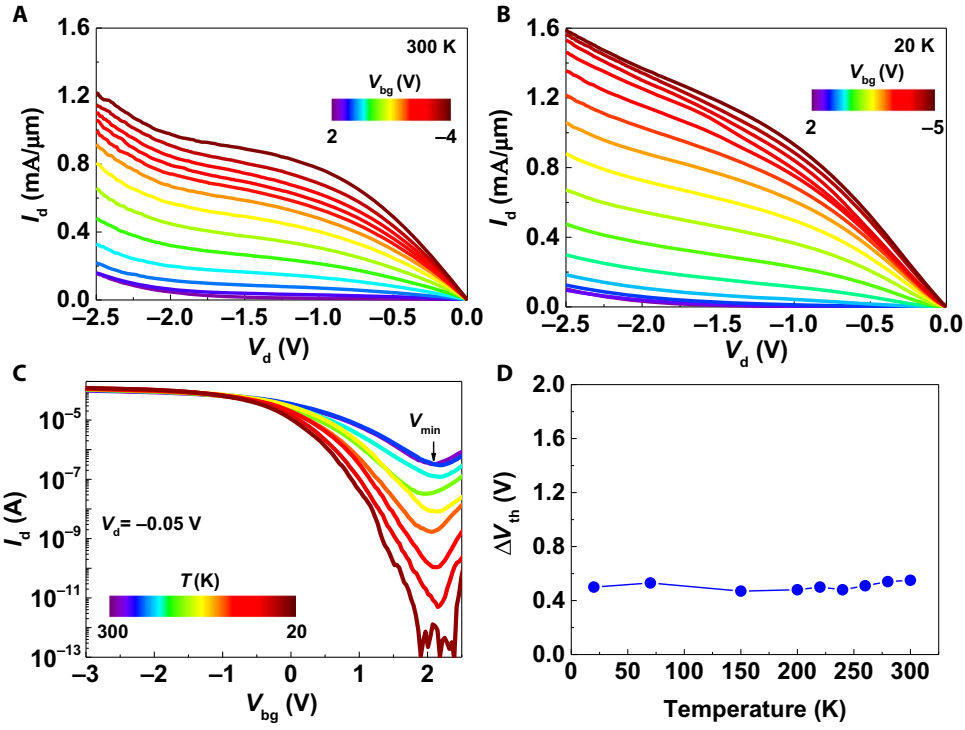

Fig. 2. Transport properties of a BP transistor at low temperature. (**A**) Output characteristics of the BP device with a channel length of 100 nm at 300 K. (**B**) Output characteristics of the same device at 20 K. (**C**) Transfer characteristics of the 100-nm device for BP on HfLaO at different temperatures. (**D**) Hysteresis values of the 100-nm device for BP on HfLaO as a function of temperature.

where V_{gs} is the gate-to-source voltage, V_t is the threshold voltage, and V'_d is the intrinsic drain-to-source voltage (*16*, *17*). The lateral field can be calculated by

$$F = \frac{V'_d}{L} = \frac{V_d - 2I_d R_c}{L} \quad (2)$$

where contact resistance R_c was measured at various carrier densities using the transfer length method, as shown in fig. S4. To obtain saturation velocity υ_{sat}, we fit velocity data in Fig. 2A to the Caughey-Thomas model

$$\upsilon_d = \frac{\mu F}{\left[1 + \left(\frac{\mu F}{\upsilon_{sat}}\right)^{\gamma}\right]^{1/\gamma}} \quad (3)$$

where μ is the mobility derived from the slope of υ_d versus F, and γ and υ_{sat} are two free-fitting parameters (*16*, *17*). We found that the value of γ changes with temperature and carrier density ranging from 0.7 to 1.8. It is clear that the fitting curves (solid line) agree well with the experimental data (scatters) at 300 and 20 K, as shown in Fig. 3A. Figure 3B shows the extracted saturation velocity versus temperature at various carrier densities. As expected, saturation velocity increases with lower carrier density, up to 1.5×10^7 cm/s at a hole density of -1.1×10^{12} cm^{-2}. In addition, saturation velocity increases with decreasing temperature because of the lower optical phonon occupation ratio at low temperature, in agreement with previous studies on BP (*11*). Figure 3C benchmarks the hole saturation velocity of BP FETs in this work with monolayer WSe_2 (p-type) as well as other common p-type bulk semiconductors (*11*, *18*–*22*). BP exhibits the highest hole saturation velocity among all semiconductors. High V_{sat} and a decent bandgap of thin BP films provide the potential for BP as a promising 2D material for future high-speed electronic and optoelectronic applications.

Theoretical modeling of ballistic transport in BP FETs

To better understand the carrier transport in the short-channel BP devices, we adopted the MIT Virtual Source (MVS) model to extract the transport parameters (*23*). The model was developed on the basis of the Landauer theory and has been successfully used in describing quasi-ballistic transport in many types of nanoscale transistors (*23*–*25*). According to the model, the saturation drain current (i.e., on current) of a nanoscale transistor can be expressed by

$$I_d = WQ_{x0}F_{sat}v_{x0} \quad (4)$$

where W is the device width, Q_{x0} and v_{x0} are carrier density and saturation injection velocity at the virtual source point (x_0), respectively, and F_{sat} is a semiempirical function to model the transition from the saturation region to the linear region. The ballistic limit injection velocity $v_T = (2k_BT/\pi m^*)^{1/2}$, where m^* is the effective mass.

Figure 4A shows the modeling results of the output *I*-*V* curves under room temperature, which agree well with experimental data. The extracted ballistic efficiency B_{sat} of the fabricated 100-nm device is as high as 36.3%. To further investigate the potential of the near-ballistic transport of our devices, we show the electronic transport results at 20 K in Fig. 4B. The extracted B_{sat} and v_{x0} for the fabricated 100-nm device are 79.4% and 1.0×10^7 cm/s, respectively, which are the record values for transistors based on 2D semiconductor materials so far. With the

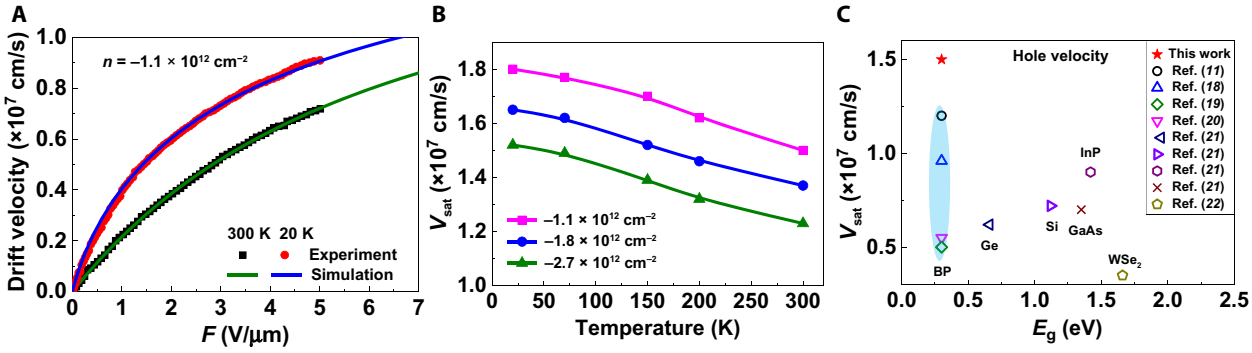

Fig. 3. Saturation velocity of BP FETs. (**A**) Drift velocity as a function of transverse electric field in the channel for the 100-nm channel length BP device at 300 and 20 K. Scatters are experimental data; solid lines are fits to and extrapolation from Eq. 4. (**B**) Extracted saturation velocity versus temperature at various hole densities. (**C**) Comparison of hole saturation velocity as a function of bandgap for different materials at room temperature.

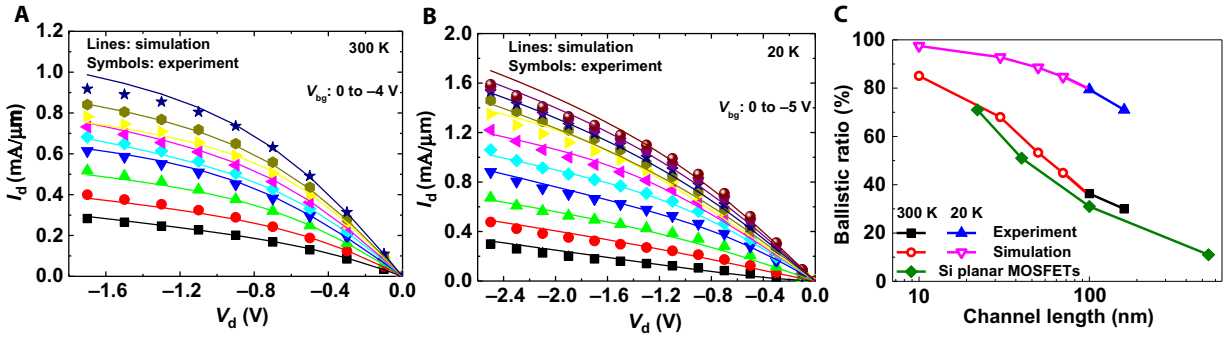

Fig. 4. Ballistic simulation of BP FETs. Comparison of the (lines) MVS model fit and (symbols) measured data for the I_d-V_d characteristics in Fig. 2. (**A**) 300 K. (**B**) 20 K. (**C**) Benchmark of ballistic efficiency in this work with Si planar MOSFETs.

obtained device parameters, model predictions for devices shorter than 100 nm at 300 and 20 K are shown in Fig. 4C. The B_{sat} increases as the channel length decreases, indicating less channel scattering events are involved in shorter channel length devices, thus resulting in higher ballistic efficiency. Compared with results at 300 K, much larger B_{sat} can be achieved in short-channel devices at 20 K, which are very close to the ballistic limit, where theoretical modeling shows that full ballistic transport can be achieved once the channel length is scaled down to 10 nm. Furthermore, the ballistic ratio of BP FETs at 300 K is always higher than that of Si metal oxide semiconductor FETs (MOSFETs) at the same channel length, as shown in Fig. 4C (*26*, *27*). Thus, our results indicate the remarkable potential of the BP-based transistors for future high-performance, high-frequency applications.

CONCLUSIONS

In summary, we have demonstrated ballistic transport of few-layer BP FETs with HfLaO dielectrics as the back gate substrate and performed theoretical modeling to gain insight into ballistic transport mechanisms. A record-high on-current density of 1.2 mA/μm at 300 K and 1.6 mA/μm at 20 K is achieved, which is mainly attributed to the high-quality HfLaO films, the excellent interface between HfLaO and BP, and the ultrahigh electrostatic doping to form low R_c. A record-high field hole saturation velocity of BP FETs of 1.5×10^7 cm/s at 300 K can be obtained. The ballistic transport behavior of the BP short-channel device is assessed by the MVS model, demonstrating a ballistic efficiency of 79.4% at 20 K. All these results make few-layer BP a very promising candidate material for future applications in high-speed electronics and optoelectronics.

MATERIALS AND METHODS

Back-gated devices

The HfLaO layer was deposited by an atomic layer deposition system (Beneq TFS 200) at 300°C. $Hf[N(CH_3)(C_2H_5)]_4$ and $La(({}^iPr_2N)_2CH)_3$ were used as precursors for HfO_2 and La_2O_3, respectively, and ozone (O_3) served as oxygen source. The cycle ratio of HfO_2 and La_2O_3 is 8:1. The Hf and La precursor pulse times were both 0.5 s. The purge time of each precursor was 10 s. The O_3 pulse time and purge time were both 1 s. Pure N_2 (99.999%) was used as carrier gas and purge gas. The HfLaO films were annealed at 500°C for 30 s in N_2. Few-layer BP flakes were mechanically exfoliated from the purchased natural bulk BP (Smart-elements) onto an HfLaO/p^{++} Si wafer in a glove box, where the oxygen and water contents are always kept below 0.1 parts per million. All samples were sequentially cleaned by acetone and isopropyl alcohol to remove any scotch tape residue. Then, poly(methyl methacrylate) resist was spin coated on the surface of the samples in the glove box where the samples were stored in between the process steps. Other fabrication process steps included electron beam evaporation and electron beam lithography, which are mostly carried out in a high-vacuum environment with minimal transfer time in between the process steps due to the air-sensitive nature of the BP material. After defining the source/drain (S/D) area by electron beam lithography, the S/D electrode metal was deposited by electron beam evaporation of Ni/Au (20/60 nm). No annealing was performed after the

deposition of the metal contacts. The electrical characterization was carried out in a lakeshore cryogenic probe station under $<10^{-5}$ torr using an Agilent B1500A parameter analyzer.

SUPPLEMENTARY MATERIALS

Supplementary material for this article is available at http://advances.sciencemag.org/cgi/content/full/5/6/eaau3194/DC1

Additional supporting information

Fig. S1. *C-V* characteristics of HfLaO films.

Fig. S2. X-ray photoelectron spectroscopy characteristics of HfLaO films.

Fig. S3. *J-V* characteristics of thin HfLaO films.

Fig. S4. Temperature-dependent transport in BP transistors.

Fig. S5. Gate-tunable contact resistance and Schottky barrier.

Table S1. Comparison of saturation velocity for holes at room temperature.

References (*28*–*31*)

REFERENCES AND NOTES

1. X. Li, L. Yang, M. Si, S. Li, M. Huang, P. Ye, Y. Wu, Performance potential and limit of MoS_2 transistors. *Adv. Mater.* **27**, 1547–1552 (2015).
2. G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D. Neumaier, A. Seabaugh, S. K. Banerjee, L. Colombo, Electronics based on two-dimensional materials. *Nat. Nanotechnol.* **9**, 768–779 (2014).
3. L. Li, Y. Yu, G. J. Ye, Q. Ge, X. Ou, H. Wu, D. Feng, X. H. Chen, Y. Zhang, Black phosphorus field-effect transistors. *Nat. Nanotechnol.* **9**, 372–377 (2014).
4. F. Xia, H. Wang, Y. Jia, Rediscovering black phosphorus as an anisotropic layered material for optoelectronics and electronics. *Nat. Commun.* **5**, 4458 (2014).
5. Y. Du, H. Liu, Y. Deng, P. D. Ye, Device perspective for black phosphorus field-effect transistors: Contact resistance, ambipolar behavior, and scaling. *ACS Nano* **8**, 10035–10042 (2014).
6. M. Buscema, D. J. Groenendijk, S. I. Blanter, G. A. Steele, H. S. J. van der Zant, A. Castellanos-Gomez, Fast and broadband photoresponse of few-layer black phosphorus field-effect transistors. *Nano Lett.* **14**, 3347–3352 (2014).
7. J. Miao, S. Zhang, L. Cai, M. Scherr, C. Wang, Ultrashort channel length black phosphorus field-effect transistors. *ACS Nano* **9**, 9236–9243 (2015).
8. A. Allain, J. Kang, K. Banerjee, A. Kis, Electrical contacts to two-dimensional semiconductors. *Nat. Mater.* **14**, 1195–1205 (2015).
9. Y. Du, L. Yang, H. Zhou, P. D. Ye, Performance enhancement of black phosphorus field-effect transistors by chemical doping. *IEEE Electron Device Lett.* **37**, 429–432 (2016).
10. X. Li, X. Xiong, T. Li, S. Li, Z. Zhang, Y. Wu, Effect of dielectric interface on the performance of MoS_2 transistors. *ACS Appl. Mater. Interfaces* **9**, 44602–44608 (2017).
11. X. Chen, C. Chen, A. Levi, L. Houben, B. Deng, S. Yuan, C. Ma, K. Watanabe, T. Taniguchi, D. Naveh, X. Du, F. Xia, Large-velocity saturation in thin-film black phosphorus transistors. *ACS Nano* **12**, 5003–5010 (2018).
12. L. M. Yang, G. Qiu, M. W. Si, A. R. Charnas, C. A. Milligan, D. Y. Zemlyanov, H. Zhou, Y. C. Du, Y. M. Lin, W. Tsai, Q. Paduano, M. Snure, P. D. Ye, Few-layer black phosporous PMOSFETs with BN/Al_2O_3 bilayer gate dielectric: Achieving I_{on}=850 μA/μm, g_m=340 μS/μm, and R_c=0.58 kΩ·μm, in 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, 3 to 7 December 2016, pp. 5.5.1–5.5.4.
13. M. Si, L. Yang, Y. Du, P. D. Ye, Black phosphorus field-effect transistor with record drain current exceeding 1 A/mm, in 2017 75th Annual Device Research Conference (DRC), South Bend, IN, 25 to 28 June 2017, pp. 1–2.
14. R. Decker, Y. Wang, V. W. Brar, W. Regan, H.-Z. Tsai, Q. Wu, W. Gannett, A. Zettl, M. F. Crommie, Local electronic properties of graphene on a BN substrate via scanning tunneling microscopy. *Nano Lett.* **11**, 2291–2295 (2011).
15. X. Cui, G.-H. Lee, Y. Kim, G. Arefe, P. Y. Huang, C.-H. Lee, D. A. Chenet, X. Zhang, L. Wang, F. Ye, F. Pizzocchero, B. S. Jessen, K. Watanabe, T. Taniguchi, D. A. Muller, T. Low, P. Kim, J. Hone, Multi-terminal transport measurements of MoS_2 using a van der Waals heterostructure device platform. *Nat. Nanotechnol.* **10**, 534–540 (2015).
16. F. Assaderaghi, D. Sinitsky, J. Bokor, P. K. Ko, H. Gaw, H. Chenming, High-field transport of inversion-layer electrons and holes including velocity overshoot. *IEEE Trans. Electron Devices* **44**, 664–671 (1997).
17. D. M. Caughey, R. E. Thomas, Carrier mobilities in silicon empirically related to doping and field. *Proc. IEEE* **55**, 2192–2193 (1967).
18. H. Wang, X. Wang, F. Xia, L. Wang, H. Jiang, Q. Xia, M. L. Chin, M. Dubey, S.-j. Han, Black phosphorus radio-frequency transistors. *Nano Lett.* **14**, 6424–6429 (2014).
19. T. Gao, X. Li, X. Xiong, M. Huang, T. Li, Y. Wu, Optimized transport properties in lithium doped black phosphorus transistors. *IEEE Electron Device Lett.* **39**, 769–772 (2018).
20. W. Zhu, S. Park, M. N. Yogeesh, K. M. McNicholas, S. R. Bank, D. Akinwande, Black phosphorus flexible thin film transistors at gighertz frequencies. *Nano Lett.* **16**, 2301–2306 (2016).
21. R. Quay, C. Moglestue, V. Palankovski, S. Selberherr, A temperature dependent model for the saturation velocity in semiconductor materials. *Mater. Sci. Semicond. Process.* **3**, 149–155 (2000).
22. Z. Jin, X. Li, J. Mullen, K. W. Kim, Intrinsic transport properties of electrons and holes in monolayer transition-metal dichalcogenides. *Phys. Rev. B* **90**, 045422 (2014).
23. S. Rakheja, M. S. Lundstrom, D. A. Antoniadis, An improved virtual-source-based transport model for quasi-ballistic transistors—Part I: Capturing effects of carrier degeneracy, drain-bias dependence of gate capacitance, and nonlinear channel-access resistance. *IEEE Trans. Electron Devices* **62**, 2786–2793 (2015).
24. S. Datta, *Lessons from Nanoelectronics: A New Perspective on Transport* (World Scientific Publishing Co Inc, 2012), vol. 1.
25. Y. Liu, M. Luisier, A. Majumdar, D. A. Antoniadis, M. S. Lundstrom, On the interpretation of ballistic injection velocity in deeply scaled MOSFETs. *IEEE Trans. Electron Devices* **59**, 994–1001 (2012).
26. M. Choi, V. Moroz, L. Smith, J. Huang, Extending drift-diffusion paradigm into the era of FinFETs and nanowires, in 2015 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Washington, DC, 9 to 11 September 2015, pp. 242–245.
27. S. Eminente, D. Esseni, P. Palestri, C. Fiegna, L. Selmi, E. Sangiorgi, Understanding quasi-ballistic transport in nano-MOSFETs: Part II—Technology scaling along the ITRS. *IEEE Trans. Electron Devices* **52**, 2736–2743 (2005).
28. X. Li, R. Grassi, S. Li, T. Li, X. Xiong, T. Low, Y. Wu, Anomalous temperature dependence in metal–black phosphorus contact. *Nano Lett.* **18**, 26–31 (2018).
29. A. V. Penumatcha, R. B. Salazar, J. Appenzeller, Analysing black phosphorus transistors using an analytic Schottky barrier MOSFET model. *Nat. Commun.* **6**, 8948 (2015).
30. G. Arutchelvan, C. J. Lockhart de la Rosa, P. Matagne, S. Sutar, I. Radu, C. Huyghebaert, S. De Gendt, M. Heyns, From the metal to the channel: A study of carrier injection through the metal/2D MoS_2 interface. *Nanoscale* **9**, 10869–10879 (2017).
31. Y. Liu, J. Guo, Y. Wu, E. Zhu, N. O. Weiss, Q. He, H. Wu, H.-C. Cheng, Y. Xu, I. Shakir, Y. Huang, X. Duan, Pushing the performance limit of sub-100 nm molybdenum disulfide transistors. *Nano Lett.* **16**, 6337–6342 (2016).

Acknowledgments: We thank the technical support from the Center of Micro-Fabrication and Characterization, WNLO, and the Analytical and Testing Center of Huazhong University of Science and Technology. **Funding:** This work was supported by the National Natural Science Foundation of China (grant nos. 61574066, 61874162, and 61522402), the Strategic Priority Research Program of Chinese Academy of Sciences under grant no. XDB30000000 and, in part, by the Fundamental Research Funds for the Central Universities under grant 2018KFYYXJJ069 and 2019kfyXKJC014. **Author contributions:** Y.W. conceived the idea. X.L. designed and carried out the experiments. Z.Y. provided the theoretical analysis and calculations. X.X. performed AFM measurements. T.L. and T.G. contributed to the electrical measurement. R.W. and R.H. contributed to the discussion of the results. X.L., Z.Y., and Y.W. contributed to the writing of the manuscript. X.L. and Z.Y. contributed equally. **Competing interests:** The authors declare that they have no competing interests. **Data and materials availability:** All data needed to evaluate the conclusions in the paper are present in the paper and/or the Supplementary Materials. Additional data related to this paper may be requested from the authors.

Submitted 13 August 2018
Accepted 15 May 2019
Published 21 June 2019
10.1126/sciadv.aau3194

Citation: X. Li, Z. Yu, X. Xiong, T. Li, T. Gao, R. Wang, R. Huang, Y. Wu, High-speed black phosphorus field-effect transistors approaching ballistic limit. *Sci. Adv.* **5**, eaau3194 (2019).

High-speed black phosphorus field-effect transistors approaching ballistic limit

Xuefei Li, Zhuoqing Yu, Xiong Xiong, Tiaoyang Li, Tingting Gao, Runsheng Wang, Ru Huang and Yanqing Wu

Sci Adv **5** (6), eaau3194.
DOI: 10.1126/sciadv.aau3194