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Negative transconductance and negative differential resistance in asymmetric narrow bandgap 2D–3D heterostructures†

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Two-dimensional layered black phosphorus is an ambipolar narrow bandgap semiconductor with excellent electronic properties. A heterostructure can be formed when black phosphorus is combined with a narrow bandgap n-type semiconductor, which can feasibly be modulated throughout the entire bandgap for both materials in momentum space, creating unique quantum tunneling devices. In this work, a black phosphorus and narrow bandgap n-type indium arsenide heterojunction is created with a broken-gap band alignment, forming two interband tunneling windows that can be modulated electrostatically. We observe simultaneous gate-tunable band-to-band tunneling induced negative differential resistance and negative transconductance in the heterointerface and the access region edge near the gate, respectively. Compared to the stringent conditions for realizing such abrupt heterojunctions with opposite doping polarities in conventional bulk semiconductors, layered two-dimensional materials provide unique opportunities for such quantum tunneling devices. Our results represent advances in the fundamental understanding of heterojunctions and will promote future applications in advanced electronics.

Due to the urgent demand for energy conservation and low power operation, tunnel field-effect transistors (TFETs) have attracted extensive attention in the past two decades, and are considered to be the most promising steep-slope switch candidates.^{1–3} Because of their importance in energy-efficient devices since power consumption began to put circuits at risk of overheating, considerable attention has been focused on various types of tunneling systems with new materials.^{4–7} TFETs based on III–V compounds with a direct bandgap have been advancing rapidly in recent years; they can achieve various heterostructures and high on-current with supply voltages of less than 0.5 V.^{8–10} Indium arsenide (InAs) is widely

used as the channel material in III–V TFETs in combination with other materials with different band structures, and it is well known for its small electron mass and narrow direct bandgap.^{11–14} However, there are many constraints in traditional III–V based heterostructures due to lattice mismatch in the material epitaxy process. As a result, the device structures and band profile designs are always limited by the practical availability of materials. On the other hand, two-dimensional (2D) layered semiconductors have emerged in recent years due to their atomic thin property and, more importantly, the weak van der Waals (vdWs) force between the layers and the feasibility of transfer to an arbitrary substrate which enable a novel approach to building artificial vdWs heterostructures.^{15–18} Black phosphorus (BP) is a two-dimensional direct bandgap p-type dominant ambipolar semiconductor with high carrier mobility and light effective mass with a bandgap around 0.3 eV for a thickness of a few nanometers.^{19–22} Since the band-to-band tunneling (BTBT) probability decreases exponentially with effective mass (m^*) and bandgap (E_g), it is best to have smaller m^* and narrower E_g for higher on-current.²³ In such a case, both InAs and BP are ideal channel material candidates for highly efficient tunnel devices. Besides, the narrow bandgaps of BP/InAs can create a tunnel junction tunable by a small supply voltage, taking account of the electron affinity difference. Moreover, the formation of this heterostructure can be obtained by dry transfer, so the sharpness of the band edges and the band alignments at the interface are more intrinsic and clear of dopant interdiffusion.²⁴ In this work, by using InAs as the source and thin BP film as the channel, a vertical asymmetric 2D/3D heterostructure is built with broken-gap band alignment. In comparison to individual BP FETs, the BP/InAs heterostructure shows a smaller subthreshold swing (SS) benefiting from the tunnel junction. More importantly, we observe a notable negative differential resistance (NDR) and negative transconductance (NTC), systematically tunable by vertical and transverse electric fields, which is difficult to achieve simultaneously in other heterostructures.^{5,25}

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Results and discussion

The BP flakes were mechanically exfoliated and then transferred to the vicinity of the InAs and insulating HfO_2 using a pick-and-place dry transfer technique.²⁶ BP was placed on top of InAs forming a vertical source–channel junction; thus the gate electric field is aligned with the tunneling direction, which can increase the tunneling probability and decrease the subthreshold slope with enhanced electrostatic control.^{12,27} The gate dielectrics were deposited by a combination of 2 nm e-beam evaporated then oxidized aluminum followed by 10 nm of HfO_2 deposited by atomic layer deposition (ALD) at low temperature (90 °C). The $\text{Al}_2\text{O}_3/\text{HfO}_2$ stack allows a low gate leakage current and high-quality BP/high- κ interface.²⁸ A three-dimensional schematic view of the BP/InAs heterostructure device is shown in Fig. 1a, where Ti and Ni were chosen to form contacts with a lower barrier for electron and hole injection into the InAs and BP, respectively.

Fig. 1b presents Raman spectra with a laser wavelength of $\lambda = 532$ nm fixed separately on the InAs, BP and their overlapped region. Raman spectra of the individual InAs substrate contain only one peak at 240 cm^{-1} , which is related to the InAs longitudinal optical (LO) phonon mode.²⁹ The typical spectra of BP comprise three distinct peaks at 363 cm^{-1} , 440 cm^{-1} , and 468 cm^{-1} , which are attributed to A_{1g}^* , B_{2g} and A_{2g}^* phonon modes, respectively.³⁰ The Raman peaks of both the individual BP and the overlapping region are almost identical, as shown in Fig. 1b. However, the intensity of the LO phonon mode of InAs is significantly reduced due to the strong interlayer electronic coupling, indicating the formation of a BP/InAs p–n junction. In addition, the Raman spectra of InAs split into two peaks located at 233 cm^{-1} and 240 cm^{-1} . We attribute the appearance of the low-frequency peak

(233 cm^{-1}) to be the result of electron accumulation at the InAs surface induced by the large electron affinity difference between BP and InAs. A similar phenomenon has been observed previously in samples of InAs with higher n-doping concentrations,^{29,31} similar to the higher electron density at the InAs surface in this work. A high resolution scanning transmission electron microscope (STEM) image of the cross-section of the BP/InAs device is presented in Fig. 1c, which clearly reveals the layered BP, the InAs crystal and the presence of a thin amorphous layer with a thickness of ~ 2.5 nm. We further performed energy-dispersive X-ray spectroscopy (EDX) elemental mapping and line-scanning to verify the material composition of the interfacial layer, as shown in Fig. 1d and e. There is a small amount of oxygen at the BP/InAs interface, which would be attributable to the formation of native oxide (PO_x or InAsO_x) due to the easily oxidizable properties of both BP and InAs.^{14,32}

Fig. 2a depicts the transfer characteristics of the individual BP FET and BP/InAs heterostructure with V_{ds} ranging from -0.2 V to -1 V with a step of -0.2 V, where in the heterostructure, the end BP is denoted as the drain side and InAs is grounded as the source. It should be noted that both structures share the same BP flake for a fair comparison. The thickness of the BP flake in this device is around 11 nm, as measured by atomic force microscopy (AFM). The transfer curves of BP FET show a typical p-type dominated ambipolar conduction behavior. However, we observe a p-type dominant transport for the BP/InAs device, as shown by the reddish line in Fig. 2a. At a positive gate bias, the drain current is almost constant and shows no modulation with gate voltage, a remarkable difference to the BP FET. The BP FET exhibits ambipolar electrical transport due to its small band gap and Fermi level pinning at the Ni contacts. The observed unipolar properties of the BP/InAs device could be attributed to carrier depletion at a positive gate voltage at the BP/InAs interface under a reverse bias. Energy band diagrams, based on numerical simulations using the nextnano software,^{33,34} are employed to interpret the cause of the difference. The calculated 2D energy band surface of the BP/InAs heterostructure is shown in Fig. 2d, and the details of the simulation can be found in ESI section 3.† The energy band alignment at the BP/InAs interface is a type-III broken-gap where the valence band maximum (VBM) of BP is above the conduction band minimum (CBM) of InAs, which meets the band alignment requirement for efficient band-to-band tunneling. The distinct electron affinity difference gives rise to the accumulation of holes in BP and of electrons in InAs near the interface, which is consistent with the Raman results discussed above. Fig. 2b shows the extracted SS *versus* drain current for both types of devices with $V_{ds} = -0.2$ V. In comparison to the BP FETs where SS is around 550 mV dec^{-1} , the BP/InAs device shows a much steeper SS of 250 mV dec^{-1} , a 120% enhancement. In addition, the change in the drain current in the subthreshold region just spans about one order of magnitude for the BP FET, while it spans at least two orders for the BP/InAs device with an SS below 800 mV dec^{-1} . This enhancement can be attributed to

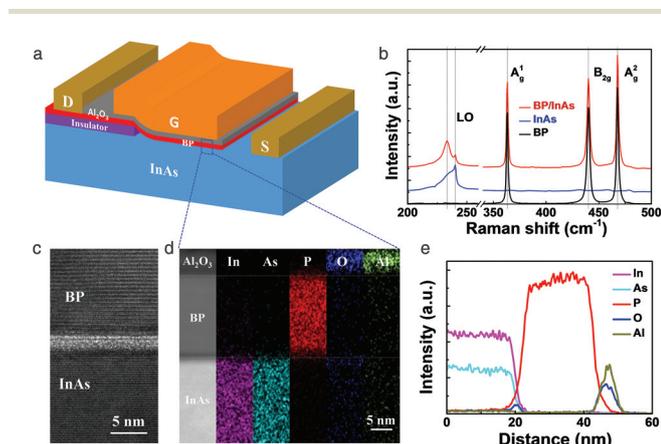


Fig. 1 Structure and material characterization of the BP/InAs heterostructure. (a) A three-dimensional schematic view of the BP/InAs heterostructure. (b) Raman spectra with a laser wavelength of $\lambda = 532$ nm fixed on the InAs, BP and their overlapped region, respectively. (c) Cross-sectional STEM image of the BP/InAs interface. (d) EDX analysis with elemental mapping of In, As, P, O, and Al elements of the $\text{Al}_2\text{O}_3/\text{BP}/\text{InAs}$ structure. Scale bar: 5 nm. (e) EDX line-scans showing the profiles of the In, As, P, O, and Al elements along the cross-section of the device.

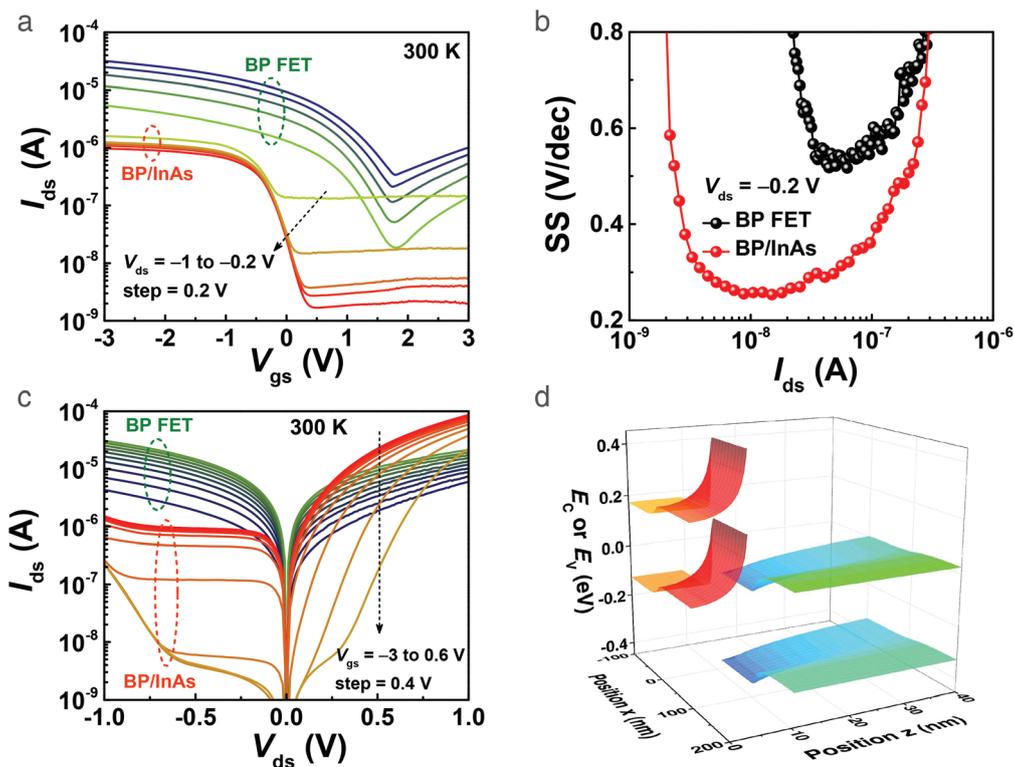


Fig. 2 Comparison of the I - V characteristics of the BP FET and BP/InAs devices at 300 K. (a) The transfer characteristics of the individual BP FET and BP/InAs heterostructure with V_{ds} ranging from -0.2 V to -1 V with a step of -0.2 V. (b) Comparison of subthreshold swing as a function of drain current with $V_{ds} = -0.2$ V. (c) The output characteristics of the two types of devices at 300 K, with V_{gs} changing from 0.6 V to -3 V with a step of -0.4 V. (d) The calculated 2D energy surface of the BP/InAs heterostructure.

the interband tunneling mechanism for the BP/InAs heterostructure with respect to the thermionic operation for a BP FET. The SS in the BP/InAs device is greater than 60 mV dec^{-1} at room temperature due to the high density of interface states at the BP/high- κ interface and can be improved by proper surface passivation and equivalent oxide thickness (EOT) scaling. In addition, the thermally stimulated current may be another reason for the large SS due to the narrow bandgap of both BP and InAs.

Fig. 2c shows the measured I_{ds} as a function of the applied V_{ds} at different gate biases for two types of devices. The individual BP FET shows a symmetric behavior at a positive or negative drain bias, which can be attributed to the symmetry of the source/drain contact with BP. However, in the BP/InAs device, the current under a forward bias is much higher than that under reverse bias conditions, resulting in strong rectifying behavior with a rectification ratio of about two orders of magnitude. However, according to the broken-gap band alignment, electrons will be tunneling from the edge of the valence band (E_V) of BP into the edge of the conduction band (E_C) of InAs when a reverse bias is applied. Under the circumstances, the tunneling current of this vertical heterojunction should increase continuously with a reverse bias, which would preclude such a large rectification ratio. This anomalous behavior is mainly due to the existence of the energy barrier between

the access BP region and the BP/InAs junction, as shown in Fig. S3c,† where the reverse bias creates a depletion region through the lateral junction. The commonly observed NDR under forward V_{ds} is also absent due to the relatively high thermionic current at room temperature from the small energy barriers of this structure, which will be discussed in further detail below.

To further understand the transport mechanisms of the BP/InAs device under various bias conditions, electrical transport properties at low temperatures were also studied. As shown in the temperature-dependent I_{ds} - V_{ds} curves in Fig. 3a, at $V_{gs} = -2.5$ V where BP is biased as strong p-type, there is negligible temperature dependence of the forward bias current when $V_{ds} > 0$, which is an evident sign that the current is dominated by BTBT rather than by thermionic emission. The location of the energy band of BP shifts up as the gate bias becomes more negative, which means that the broken-gap band window between BP and InAs increases continuously, as shown by the red line in Fig. 3d. In this case, the thermionic current is suppressed by the high electron barrier, and the BTBT current dominates the drain current at the BP/InAs interface. Thus, the forward current remains unchanged as the temperature decreases because of this dominant interband tunneling. However, the current under reverse bias at $-1 \text{ V} < V_{ds} < 0$ reduces by about 10 times as the temperature decreases from

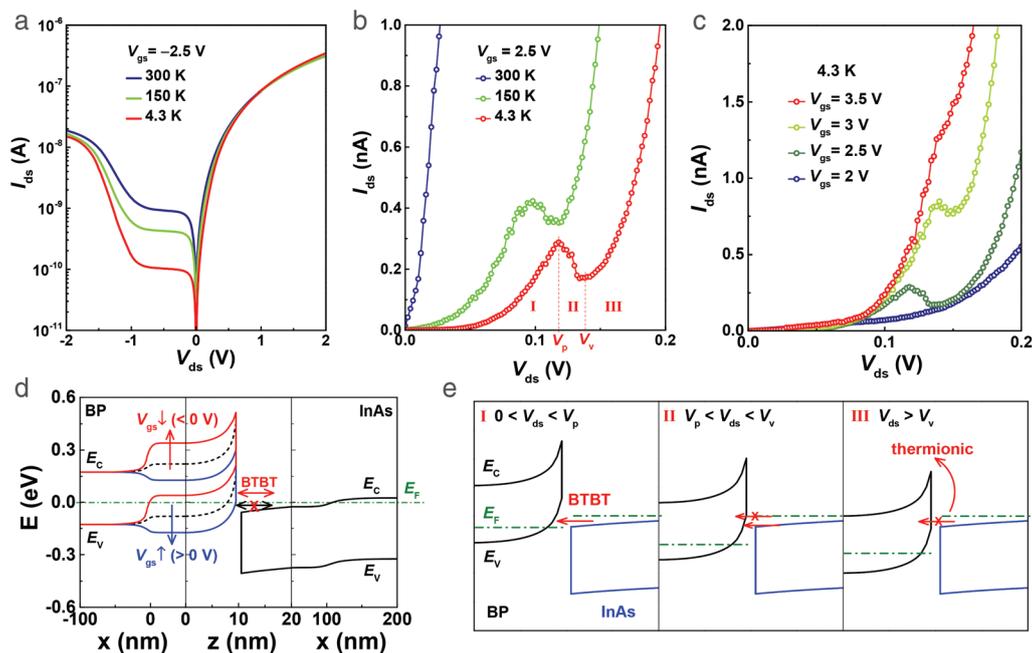


Fig. 3 NDR properties of the BP/InAs heterostructure. (a) The temperature-dependent I_{ds} - V_{ds} curves with $V_{gs} = -2.5$ V. (b) The temperature-dependent I_{ds} - V_{ds} with $V_{gs} = 2.5$ V. An increasingly apparent NDR effect was observed with temperature decreases in the forward characteristics. (c) The I_{ds} - V_{ds} curves with different gate biases at 4.3 K. (d) The energy band transition under positive and negative gate biases. (e) The energy band diagrams perpendicular to the BP/InAs heterojunction under three different bias conditions.

300 K to 4.3 K, indicating that the barrier between the access region and the BP/InAs junction plays an essential role in carrier transport, as mentioned above, where thermionic transport dominates. At even larger negative drain bias beyond -1 V, the barrier for holes at the BP side is gradually eliminated from the lateral electric field. Thus, the reverse currents increase exponentially and the temperature dependence continues to weaken, and interband tunneling takes over again, similar to the drain induced barrier lowering effect.

Fig. 3b shows I_{ds} - V_{ds} at $V_{gs} = 2.5$ V for the same device measured at three different temperatures. We observe an increasingly apparent NDR effect when the temperature decreases under forward bias, which further confirms the existence of BTBT at the BP/InAs junction, consistent with previous tunneling devices.^{7,25,35} As discussed above, the absence of NDR behavior at room temperature is mainly due to the coexistence of both the BTBT current and the thermionic current, and the latter dominates. However, at low temperatures, the thermionic current is suppressed and interband tunneling dominates, as shown by the green and red curves at 150 K and 4.3 K in Fig. 3b, which exhibit the typical I - V characteristics of an Esaki tunnel diode. Note here that the gate leakage current is negligible compared with the drain current in the BP/InAs device. Moreover, this NDR behavior can be observed for both voltage sweep directions, as shown in Fig. S4a.† The NDR effect under forward bias conditions can be explained in terms of interband tunneling, as shown in the band diagram in Fig. 3e. In region I, as the V_{ds} is increased up to the voltage V_p , the interband tunneling current continues to

increase. In region II, as the conduction band edge in the InAs side becomes uncrossed with the valence band edge in the BP side, the current decreases because of the lack of allowed states of corresponding energies for tunneling. The small peak and valley voltages indicate that the tunneling window is quite narrow (~ 0.1 V). In region III, when V_{ds} exceeds V_v , the thermionic current will dominate, as in the case of the usual p-n diode.

Fig. 3c shows I_{ds} - V_{ds} curves with four typical gate biases at 4.3 K, where the NDR behavior is clearly gate controllable under forward V_{ds} , which can be attributed to the effective modulation of the doping density in the BP channel under electrostatic control. The larger positive gate bias decreases the energy band edge of BP, and the BTBT window at the BP/InAs interface narrows and eventually disappears, resulting in a decreasing trend of the peak-to-valley ratio (PVR). When the valence band of BP eventually shifts to below the conduction band of InAs, there are no available states in BP opposite to the filled states in InAs and the tunneling current diminishes. The energy band transition is shown by the blue line in Fig. 3d.

Fig. 4a shows the double sweep transfer characteristics of the BP/InAs device under reverse bias at 4.3 K. The drain current increases at a more negative gate voltage at first. Interestingly, instead of a monotonic current increase, the drain current decreases sharply when V_{gs} decreases further and then slowly increases after the valley at even more negative V_{gs} . This non-monotonic dependence induces a sign change in transconductance, resulting in negative transconductance

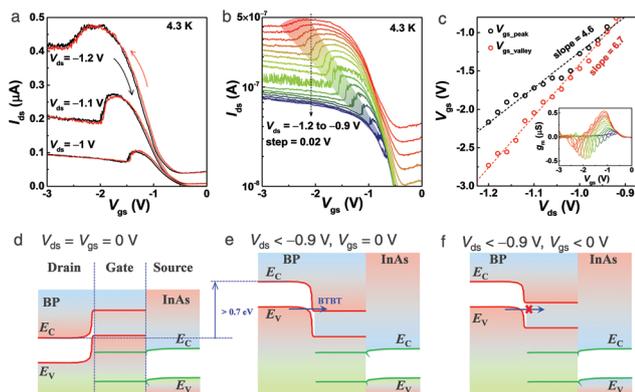


Fig. 4 NTC features of the BP/InAs heterostructure. (a) The linear transfer characteristics under three different V_{ds} of the BP/InAs device at 4.3 K. A pronounced NTC behavior was observed. (b) The detailed transfer curves under various negative drain biases in a semi-log scale. (c) The V_{gs} corresponding to the current peaks and valleys as a function of V_{ds} , indicating a linear dependence with slopes of 4.6 and 6.7, respectively. (d), (e) and (f) The energy band diagrams along the lateral directions of the BP/InAs interface under different bias conditions.

(NTC), which has been observed previously from the superlattice effect in III-V resonant tunneling devices.³⁶ In addition, this NTC behavior is robust and repeatable at both forward and reverse sweeps. As reverse bias in the heterojunction moves more negatively, the barrier between the BP access region and the BP/InAs junction at the drain side will be gradually eliminated. When the applied reverse drain voltage increases further beyond -0.9 V, the E_V of BP at the drain side will be pulled up beyond the E_C of BP at the BP/InAs junction, under which the energy band diagram will then form a tunneling window available at the gate access region and the heterojunction. For a fixed V_{ds} , the negative gate bias can modulate the BP energy band of the heterojunction to tune the overlap region of the available tunneling states, and the current will decrease with NTC behavior once the tunneling current has been eliminated. At more negative drain biases, the available states for tunneling are larger and create a larger tunable range for the gate bias V_{gs} . As shown in the corresponding energy band transitions in Fig. 4d–f, the observed NTC phenomena occur only at a large reverse drain bias (< -0.9 V), which is consistent with the required band offset of more than 0.7 eV.

Fig. 4b shows a systematic study of the transfer curves under a series of negative drain biases in the semi-log scale. The positions of the current peak and valley shift to the more negative gate bias and the voltage spans between peak and valley continuously enlarge as the reverse drain bias increases, which are indicated by the shaded region in Fig. 4b. Fig. 4c shows the position of V_{gs} corresponding to the current peak and valley as a function of V_{ds} , indicating a linear dependence with slopes of 4.6 and 6.7, respectively. This can be attributed to the fact that a larger negative V_{ds} will pull up the energy band of the access BP further with regard to the channel BP, and therefore it will need a larger V_{gs} to eliminate the tunnel-

ing window within BP. The inset of Fig. 4c shows the transconductance g_m as a function of V_{gs} at various V_{ds} , exhibiting a near symmetric positive and negative transconductance. The sign change in transconductance is particularly useful for multivalued logic circuits, which have been studied in previous work.^{34,37}

Conclusions

In summary, we have demonstrated a unique interband tunneling device based on a narrow bandgap 2D–3D BP/InAs vertical heterojunction, which was connected in series right next to a drain field controlled BP access region, simultaneously exhibiting unique negative differential resistance and negative transconductance behaviors. These behaviors can be tuned continuously by both gate voltage and drain voltage, with a detailed mechanism analysis using band diagram simulations. The results of the BP/InAs heterostructure have significance in both scientific understanding and technological applications of the tunneling device.

Methods

We start with an InAs wafer and deposit 20 nm of Ti/60 nm Au as the ohmic contact to InAs using e-beam evaporation (EBE). Then, 20 nm of insulating dielectric HfO_2 was deposited at 250 °C by atomic layer deposition (ALD), followed by rapid thermal annealing (RTA) at 500 °C for 30 s in a nitrogen ambient atmosphere to improve the dielectric film quality. Next, the 20 nm HfO_2 /InAs wafer was patterned using photolithography and the dielectric HfO_2 was etched using inductively coupled plasma (ICP). After the BP flakes were exfoliated and transferred onto the substrate, a stack of 20 nm Ni/60 nm Au was deposited as the BP contact. Then, to minimize surface impurities and traps at the BP/high- κ interface, we adopted two steps for the critical processing step of the gate dielectrics. First, 2 nm of Al was deposited directly on the BP using e-beam evaporation, and about 5 nm thin oxide of Al_2O_3 was formed by native oxidation of Al. Second, 10 nm of HfO_2 was deposited by ALD at low temperature (90 °C) to minimize the thermal budget of the BP crystal. The Al_2O_3 / HfO_2 stack allows for an extremely low gate leakage current and high-quality BP/high- κ interface. Finally, a stack of 20 nm Ni/60 nm Au gate electrode was deposited to complete the device. All measurements were performed using the LakeShore cryogenic probing system, which enables a vacuum and cryogenic measuring environment. The I - V characterizations were measured using an Agilent B1500A semiconductor parameter analyzer. The TEM images and the energy dispersive X-ray analysis were performed using a field-emission TEM (Talos F200S).

Conflicts of interest

There are no conflicts to declare.

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