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Large, Tunable Magnetoresistance in Nonmagnetic III–V Nanowires

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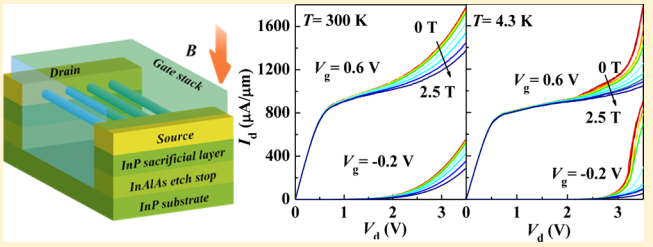
Supporting Information

ABSTRACT: Magnetoresistance, the modulation of resistance by magnetic fields, has been adopted and continues to evolve in many device applications including hard-disk, memory, and sensors. Magnetoresistance in nonmagnetic semiconductors has recently raised much attention and shows great potential due to its large magnitude that is comparable or even larger than magnetic materials. However, most of the previous work focus on two terminal devices with large dimensions, typically of micrometer scales, which severely limit their performance potential and more importantly, scalability in commercial applications. Here, we investigate magnetoresistance in the impact ionization region in InGaAs nanowires with 20 nm diameter and 40 nm gate length. The deeply scaled dimensions of these nanowires enable high sensibility with less power consumption. Moreover, in these three terminal devices, the magnitude of magnetoresistance can be tuned by the transverse electric field controlled by gate voltage. Large magnetoresistance between 100% at room temperature and 2000% at 4.3 K can be achieved at 2.5 T. These nanoscale devices with large magnetoresistance offer excellent opportunity for future high-density large-scale magneto-electric devices using top-down fabrication approaches, which are compatible with commercial silicon platform.



KEYWORDS: *Magnetoresistance, impact ionization, nanowire, transistor, InGaAs*

The effect of magnetoresistance (MR) has been widely used in applications such as high-density information storage, biochips, and magnetic sensors,[1−5] and these applications are predominately based on magnetic materials. Recently, research efforts have been made on magnetoresistance in nonmagnetic semiconductors,[6−12] as they provide similar or larger sensitivity to magnetic fields than magnetic materials.[13−15] These magnetic field dependent resistances mostly originate from orbital motion of charged carriers, hole−electron "resonance", quantum confinement, spin−spin interaction, or inhomogeneity such as the space-charge effect.[7−9,16] These devices with shrinking channel dimensions also provide a great opportunity to study weak localization effects and quantum confinement effects.[17−22] In the past few years, a different approach based on magnetic suppression on impact ionization has been reported in silicon and other materials, where Lorenz forces effectively increase the travel lengths of electrons and reduces their energy.[23−27] However, most of these MR devices are micrometer planar devices, limiting their use in modern high density electronic industry which is quickly approaching tens of nanometers. In addition, the modulation of carrier transport by Lorenz forces is ineffective in these large planar devices, especially under vertical magnetic fields. Moreover, the MR of the predominating two-terminal pn junction devices cannot be tuned, and thus precise control of both doping profile and carrier injection is required. To increase the compatibility with modern integrated circuits, multiterminal reproducible magnetic devices are highly demanded.[23] $In_{0.65}Ga_{0.35}As/In_{0.53}Ga_{0.47}As$ is a high mobility compound semiconductor with a bandgap ∼0.6 eV and an electronic effective mass ∼0.041 times of that of a free electron. MR devices based on $In_{0.65}Ga_{0.35}As/In_{0.53}Ga_{0.47}As$ gate-all-around (GAA) nanowire with 40 nm gate length studied here not only scale the physical dimensions more than 3 orders of magnitude but also introduce a ultraeffective electrostatic control which modulates the MR through carrier density.

$In_{0.65}Ga_{0.35}As/In_{0.53}Ga_{0.47}As$ GAA nanowire transistors are fabricated with 20 nm width, 30 nm height, and 40 nm gate length using standard top-down fabrication approach by electron beam lithography.[28,29] Detailed material compositions of a single InGaAs nanowire are shown in the schematic view in Figure 1a. Each InGaAs channel consists of a 10 nm $In_{0.53}Ga_{0.47}As$ layer sandwiched by two 10 nm $In_{0.65}Ga_{0.35}As$ layers to boost the channel mobility and reduce the interface trap density. The $In_{0.65}Ga_{0.35}As/In_{0.53}Ga_{0.47}As$ channel is lightly doped at around 2×10^{16} cm^{-3}. Figure 1b depicts the schematic of the InGaAs nanowire metal−oxide−semiconductor field effect transistor (MOSFET). Each device is integrated with four parallel nanowires. The nanowires were formed using ICP plasma etching followed by selective wet etching which removed the underlying InP layer. Then the nanowires were

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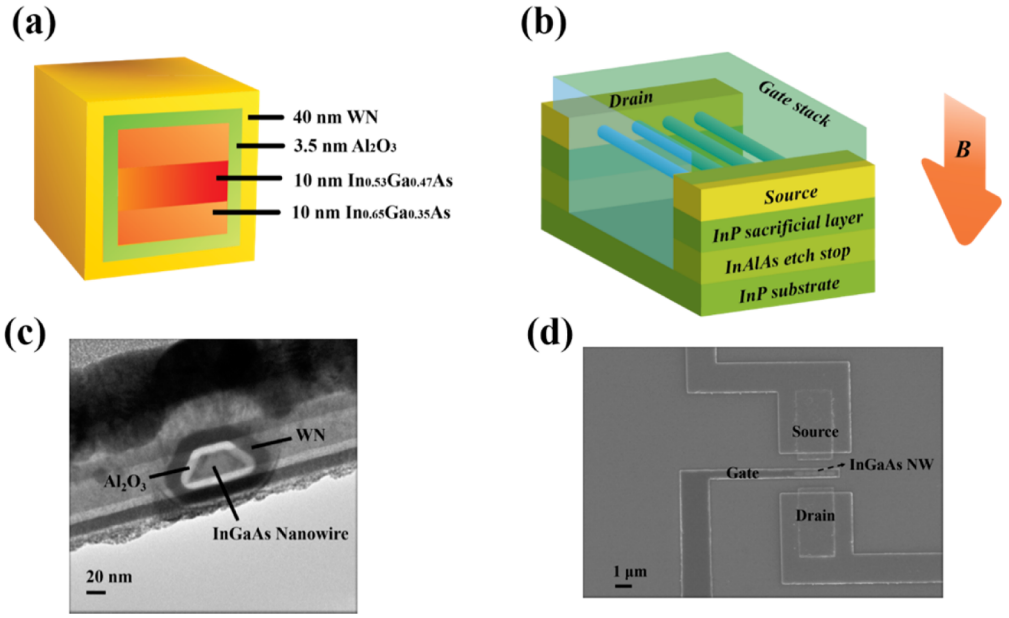

Figure 1. $In_{0.65}Ga_{0.35}As/In_{0.53}Ga_{0.47}As$ gate-all-around nanowire transistors schematics. (a) The cross-sectional view of InGaAs nanowires with ALD Al_2O_3/WN gate-stack. (b) Schematic of the gate-all-around nanowire InGaAs FET. The surrounding gate dielectric is 3.5 nm Al_2O_3. (c) TEM image of the cross section of InGaAs nanowires. (d) SEM image of parallel InGaAs nanowires in the MOSFET.

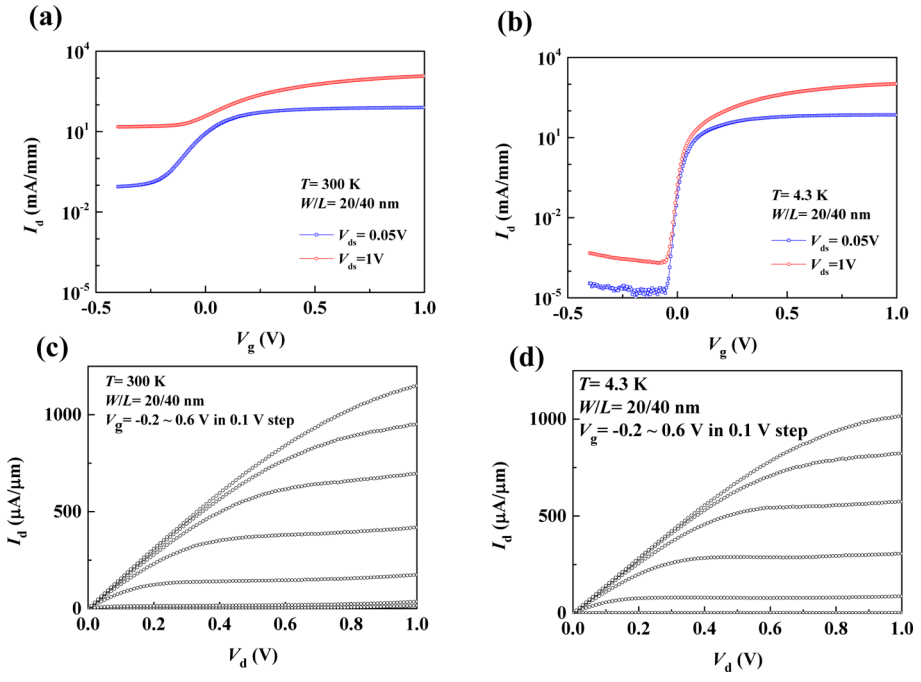

Figure 2. Transfer and output characteristics of a 40 nm $In_{0.65}Ga_{0.35}As/In_{0.53}Ga_{0.47}As$ FET at different temperatures. Transfer characteristics of the device at temperatures at 300 K (a) and 4.3 K (b) with V_d = 0.05 and 1 V. Output characteristics of the device at 300 K (c) and 4.3 K (d).

wrapped by 3.5 nm Al_2O_3 and WN high-*k*/metal gate stacks deposited by atomic layer deposition (ALD) as shown in the TEM image of Figure 1c. Due to a positive slope ~60° of the etching sidewall, the actual nanowire top width is 20 nm, and the bottom width is 55 nm. The finished InGaAs FET with four parallel nanowires is confirmed by the SEM image as shown in Figure 1d. Details of the device process are discussed in the Methods. The magnetic field applied in our study is always perpendicular to the substrate. The drain current, I_{ds}, was measured with or without the magnetic field from room temperature down to 4.3 K.

Transfer characteristics at room temperature and 4.3 K of a 40 nm long device at both linear and saturation region are shown in Figure 2a and b, respectively. As temperature decreases, the subthreshold slope changes from 108 mV/decade at 300 K to 11 mV/decade at 4.3 K, drain induced barrier lowering changes from 115 mV/V to 6 mV/V, and the on−off ratio also improves from 43 at 300 K to 1.8×10^6 at 4.3 K. Figure 2c and d shows the typical output characteristics of this device at 300 and 4.3 K, and the on-current is slightly reduced at 4.3 K mainly because of the increase of contact resistance as temperature reduces. Hot carriers gain their

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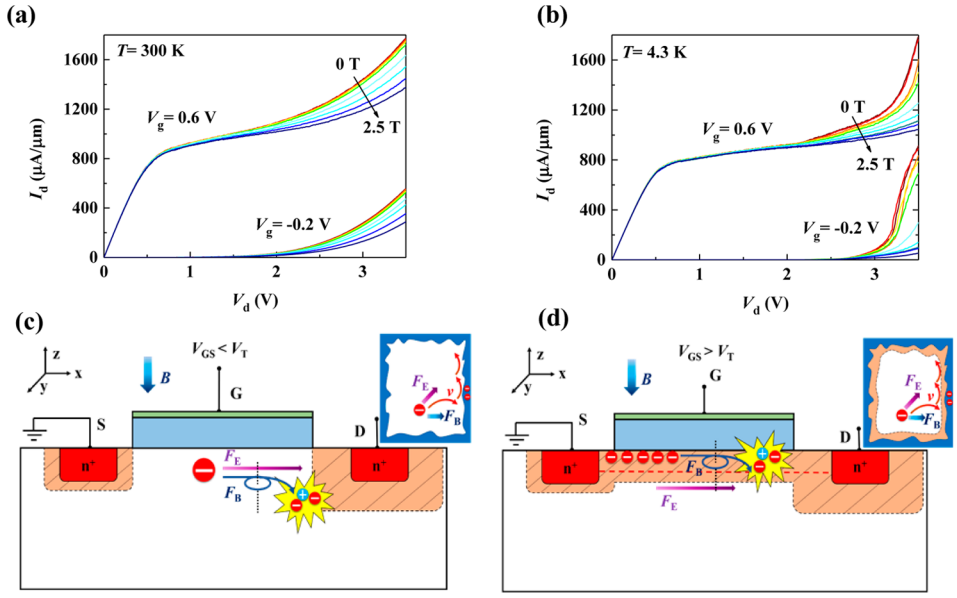

Figure 3. Transport characteristics of a 40 nm $In_{0.65}Ga_{0.35}As/In_{0.53}Ga_{0.47}As$ FET at depletion and strong inversion region. Output characteristics of the device at 300 K (a) and 4.3 K (b) with gate−source voltage of −0.2 and 0.6 V under various magnetic fields from 0 to 2.5 T. Schematic diagrams illustrating transport mechanism in depletion (c) and inversion region (d).

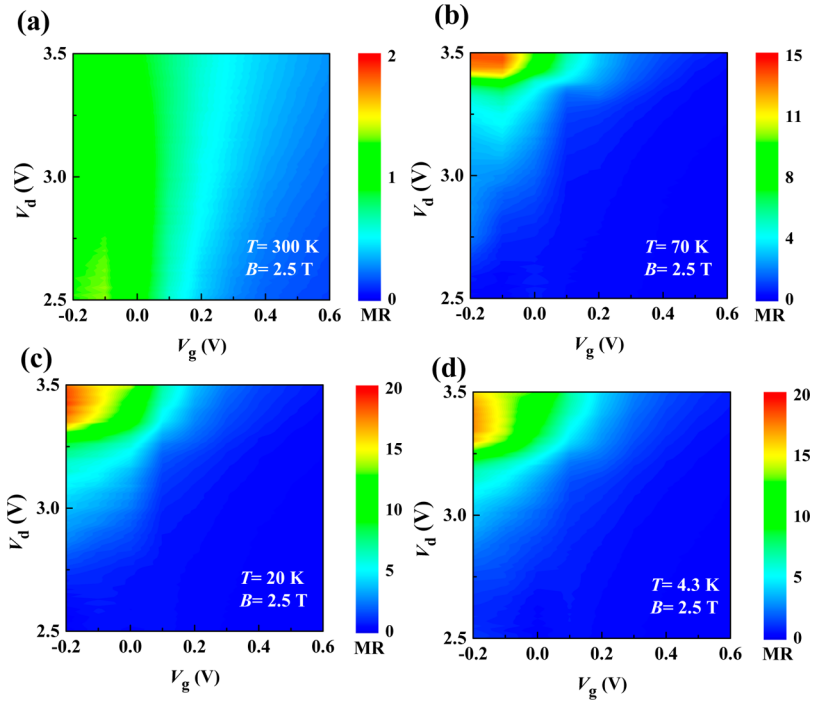

Figure 4. Contour plot of magnetoresistance of the $In_{0.65}Ga_{0.35}As/In_{0.53}Ga_{0.47}As$ FET as a function of transverse and vertical electric fields. Magnetoresistance measurements as a function of drain−source bias and gate voltage at 300 K (a), 70 K (b), 20 K (c), and 4.3 K (d) at 2.5 T.

kinetic energy via the acceleration process under a high lateral electric field, which is relatively feasible in our short channel. As shown in Figure 3a, when drain voltage exceeds 2 V, the drain current deviates from the typical current saturation and starts to increases nonlinearly with drain voltage. When kinetic energy of electrons is sufficiently high, these hot carriers can ionize neutral centers and generate electron−hole pairs which will be separated quickly by the large electric field. Moreover, the recombination rate is smaller under high electric fields since the capture cross section decreases with increasing carrier energy.[30] When the electric field exceeds a certain critical value, the ionization rate is greater than the recombination rate, which produces large amount of electron−hole pairs followed by a sharp increase of electric current. This behavior persists as the temperature is reduced down to 4.3 K as shown in Figure 3b, except that the onset drain voltage of the impact ionization increases, which is expected due to the increase of the contact resistance.

The impact ionization in the nanowire devices can be effectively tuned by applying a magnetic field as shown in Figure 3a and b, where the impact ionization is significantly suppressed under a magnetic field of 2.5 T even at the highest

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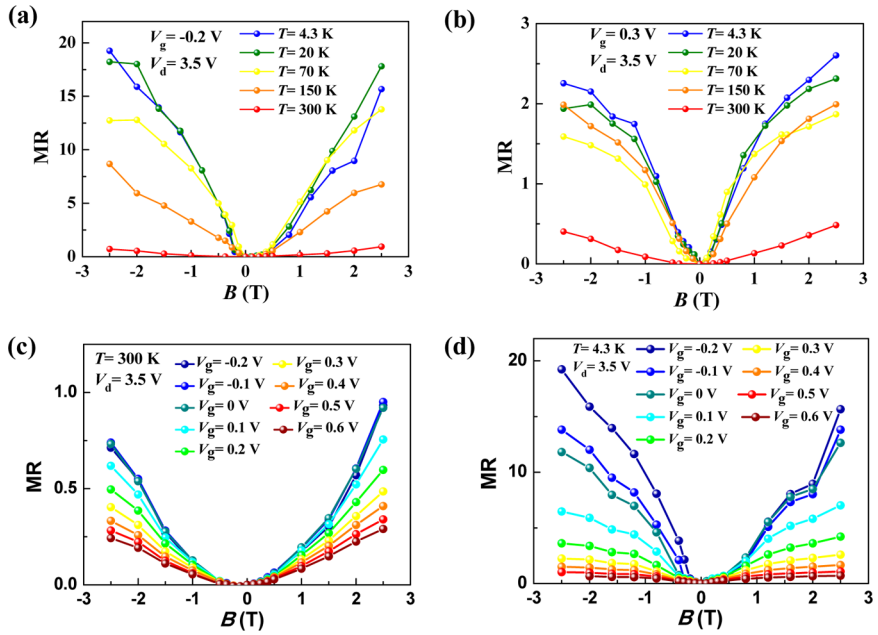

Figure 5. Linear and symmetric magnetoresistance in $In_{0.65}Ga_{0.35}As/In_{0.53}Ga_{0.47}As$ nanowire FET tuned by gate bias and temperatures. Magnetoresistance as a function of magnetic field with gate−source bias of −0.2 V (a) and 0.3 V (b) under temperatures of 4.3, 20, 70, 150, and 300 K. Magnetoresistance as a function of magnetic field under temperatures of 300 K (c) and 4.3 K (d) with gate−source bias ranging from −0.2 to 0.6 V.

drain bias of 3.5 V. An applied magnetic field poses large Lorenz force to the carriers with high velocity in the impact ionization regime where carriers deviate from the electric field direction with more inelastic scattering, and this process effectively increases the on-set voltage of the impact ionization as shown in Figure 3c and d. Moreover, because of the novel nanowire structure of our devices, these carriers undergo more surface roughness scattering when they travel near the interface of the sidewalls of the nanowires. Compared with planar devices, their kinetic energy reduces more significantly when applying a transverse magnetic field. Furthermore, the binding energy of electrons bound to impurities is increased by the applied magnetic fields. As a result, bound states are formed with binding energy which increases as the magnetic field rises due to decreasing overlapping. The influence of the magnetic fields on binding energies depends on the comparative values between the magnetic length and radius of electronic wave.[30,31] Unlike InAs nanowires which start to show quantum confinement effects when the diameter reduces to sub-30 nm, the Fermi wavelength is around ∼26 nm for our $In_{0.53}Ga_{0.47}As/In_{0.65}Ga_{0.35}As$ with a larger electron effective mass, and as a result, quantum confinement effects can hardly be observed for InGaAs nanowires with diameter larger than 30 nm.[17−22] As can be seen in Figure 1 c, the 20 nm diameter nanowire is actually trapezoidal with top width of ∼20 nm, the bottom width of ∼55 nm, and height of 30 nm. These dimensions are larger than the carriers' Fermi wavelength, and quantum confinement effects are minimal in the radial direction. Moreover, the scattering length is smaller than the cyclotron radius which means ballistic transport is not the case either in the longitudinal or radial direction. As a result, subbands modification and its impact on MR plays a minimal role here in our devices.

Figure 3c illustrates carrier trajectory in depletion region, where n−p boundary is formed between minority (electrons) in the channel and ionized donors near the doped drain region. The inhomogeneity provided by the n−p boundary becomes sufficiently high when drain-source voltage is biased at 3.5 V. The current trajectory in the boundary region can be distorted by an applied magnetic field, resulting in large magnetoresistance. Magnetoresistance in strong inversion region shown in Figure 3d can be related to carrier avalanche. As drain−source voltage is swept toward 3.5 V, hot electrons with large kinetic energy impact with acceptors in the channel, resulting in increased electron−hole pairs. These electron-pairs are pushed by Lorentz force, being deviated from moving horizontally to the channel.

Compared to two terminal p−n junctions, an important feature of a transistor is that current can be tuned by gate voltage. Figure 4a shows the magnetoresistance as a function of V_d and V_g at a magnetic field of 2.5 T at 300 K. The magnetoresistance is defined here as $MR = [R(B) - R(B = 0)]/R(B = 0)$, where $R(B)$ is the drain−source resistance $(=V_{ds}/I_{ds})$ at magnetic field B. The observed magnetoresistance shows an increasing trend toward depletion region, which can be attributed to stronger modulation of magnetic fields in space charge region than in strong inversion region. As temperatures decrease down to 70 K (Figure 4b), the monotonic increase of magnetoresistance as V_d swept from 2.5 to 3.5 V can be clearly observed. The magnetoresistance increases at higher drain bias because the maximum magnetic field of 2.5 T can significantly suppress impact ionization. Figure 4c and d also shows the general trend that magnetoresistance is higher at lower gate bias and higher drain bias, indicating this electric-field-controlled MR device is applicable under all low temperatures. Compared with the MR device based on high mobility microsized planar InAs channel in ref 10, the MR of our InGaAs nanowire devices is smaller at room temperature and increases sharply at lower temperatures. The impact ionization rate in our work is affected by several factors including the interface traps between InGaAs and gate dielectrics, surface roughness scattering from sidewalls created by dry etching, and nonideal space charge region of the

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depleted pn junctions at source and drain area. These scatterings decrease sharply at low temperatures due to trap freezing and smaller thermal energy. At low temperatures, carrier can achieve much higher kinetic energy and impact ionization rate with greatly reduced scatterings.

To provide better understanding of the magnetic field dependence of the MR, a detailed discussion is provided in Figure 5a and b, where MR at V_d = 3.5 V at various temperatures is plotted against magnetic field for different gate voltages V_g = −0.2 V and V_g = 0.3 V, respectively. When the magnetic field increases, the MR increases linearly without saturation up to ±2.5 T. As shown in Figure 5a, impact ionization induced magnetoresistance still exhibits large amplitude at room temperature, for instance, MR = 93% at V_g = −0.2 V and B = 2.5 T. First, the band gap energy of $In_{0.65}Ga_{0.35}As/In_{0.53}Ga_{0.47}As$ tends to decrease from around 0.7 to 0.62 eV as the temperature increases from 4.3 to 300 K. A narrower band gap can increase the possibility for interband impact ionization, and this will result in smaller threshold voltage for impact ionization. Second, carrier mobility decreases at higher temperature due to increased phonon scattering. Lastly, impact ionization and thermal recombination coefficients both depend on temperatures. Higher temperatures increase ionization rate and decrease the on-set voltage for carrier avalanche. Meanwhile, the higher temperature increases excited trapping centers, resulting in reduction of thermal recombination and the excess electron−hole pairs travel with longer lifetime.[30]

As temperature drops down to 4.3 K, a large MR of 1925% can be observed at B = −2.5 T for V_g = −0.2 V. We can also observe slight asymmetry at positive half of magnetic fields. This may come from temporal instabilities of the avalanche current, which can occur at high electric fields. Figure 5b shows the linear and nonsaturation behavior remains at higher V_g, though with a reduction of magnetoresistance by a factor of 8 at the same conditions. When the temperature reduces from 300 to 4.3 K, the MR increases sharply under both gate biases. However, the amount of the increases reduces significantly at higher gate voltage where carrier density is much larger at channel inversion. As discussed above, carrier density induced by the gate voltage plays an important role in the MR devices. Figure 5c and d show magnetic field dependent MR at V_d= 3.5 V for various gate voltages from −0.2 to 0.6 V at both 300 and 4.3 K, respectively. At both temperatures, the MR increases dramatically at lower gate voltage where carrier density is smaller, which is consistent with the impact ionization ratio.

In summary, we have demonstrated extraordinarily large magnetoresistance by the suppression of impact ionization of high-mobility $In_{0.65}Ga_{0.35}As/In_{0.53}Ga_{0.47}As$ GAA nanowire transistors by applying a perpendicular magnetic field. A magnetoresistance of nearly 100% was demonstrated at room temperature and up to 1925% at 4.3 K, which can be effectively tuned by the gate bias. These results demonstrate that electrical properties of nonmagnetic narrow bandgap III−V nanowires MOSFETs are sensitive to the external magnetic fields, which leads to the potential applications as magneto-electronic devices in memory storage and magnetic sensors.

Methods. The starting material is a 30 nm lightly p-doped InGaAs channel layer, an 80 nm undoped InP sacrificial layer, and a 100 nm undoped InAlAs etch stop layer on a semi-insulating InP (100) substrate grown by molecular beam epitaxy (MBE). The InGaAs channel layer consists of 10 nm $In_{0.53}Ga_{0.47}As$ layer sandwiched by two 10 nm $In_{0.65}Ga_{0.35}As$ layers. After a 10 nm ALD Al_2O_3 was deposited as an encapsulation layer, source and drain implantation was performed using PMMA resist as mask. Dopant activation was done by rapid thermal annealing at 600 °C for 15 s in N_2 ambient. Then fin structures were defined by ICP plasma etching. HCl based solution was used to release localized nanowires. The 3.5 nm Al_2O_3/WN high-k/metal gate stacks were deposited by atomic layer deposition surrounding the nanowire channel. This ALD process is critical for realizing the GAA structure with excellent conformity and uniformity. Cr/Au gate pattern was then defined and used as hard mask for the following CF_4/Ar ICP plasma gate etching. Source and drain metal was then formed by e-beam evaporation of Au/Ge/Ni. The d.c. characterizations were carried out in a Lakeshore cryogenic probe station under 10^{-3} Torr using an Agilent parameter analyzer B1500A.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.5b03366.

Information on the tunable magnetoresistance and reproducibility of the MR devices (PDF)

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Notes

The authors declare no competing financial interest.

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