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Black Phosphorus Radio Frequency Electronics at Cryogenic Temperatures

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Black phosphorus (BP) has great potential in high-performance radio frequency electronics owing to its high carrier mobility and velocity. The electrical properties of black phosphorus experience rapid deterioration upon exposure to moisture and oxygen, which poses a challenge in the device fabrication, especially the deposition of gate dielectrics using conventional top-gate approach. Herein, a Damascene-like planarization process is presented to create an embedded gate stack with high-κ dielectrics under a gate-first approach, which minimizes surface impurities and traps at the black phosphorus/high-κ interface and preserves the high-quality black phosphorus channel. The radio frequency performances of this structure improve at least twice compared with conventional top-gate structures. A record high extrinsic f_{max} of 17 GHz at room temperature for the device with 400 nm gate-length is achieved, which further increases to around 31 GHz at 20 K. Finally, BP transistor-based mixers operating at gigahertz frequency are also demonstrated for the first time.

1. Introduction

Black phosphorus (BP) is a promising emerging material for high-performance electronic applications such as radio frequency (RF) transistors because of its excellent transport properties.[1–3] The most attractive characteristic of BP is the intrinsic high hole mobility of 10^2–10^4 cm^2 V^{-1} s^{-1}, surpassing most other 2D semiconductors including transition metal dichalcogenides.[4–9] Previously, high on-state drive current and transconductance have been achieved in BP field effect transistors (FETs).[10–12] Meanwhile, the moderate bandgap of BP would lead to excellent current saturation characteristics, which is crucial to a high power gain in RF devices. Significant progress has been made in the development of RF transistors based on both rigid and flexible substrates.[1–3] Nevertheless, previous studies show BP is unstable at ambient conditions due to its reactions with oxygen and water especially under illumination, presenting a great challenge for top-gate RF device fabrication since atomic layer deposition (ALD) typically needs oxygen or water as precursor.[13–15] Even though recent research progress of capping BP with ALD high-κ dielectrics shows effective suppression of the black phosphorus surface oxidation,[16–18] this process still degrades the electric performance of BP transistors compared with the back-gate devices with minimal exposure to precursors.[19] As shown in previous studies, electric performance of BP FETs can be dominated by the channel dielectric interface where ALD high-κ dielectrics performs better than conventional SiO_2. For instance, back-gate BP transistors on high-κ substrate exhibit improved device performance in comparison with BP FETs on conventional SiO_2.[11,20] Also, encapsulation by hexagonal boron nitride results in great enhancement of the hole mobility of BP.[6,21,22] However, this approach requires multiple dry transfer steps for both black phosphorus and hexagonal boron nitride flakes with precise alignment for a single device, and thus it has extremely low throughput and yield.

In this paper, we report a new approach toward high-performance BP RF transistors using a Damascene-like planarization process to create an embedded gate stack with high-κ dielectrics, which enables high-quality interface while avoids the precursor exposure to the BP channel surface at the same time.[23,24] Side-by-side comparison with two conventional top-gate structures shows at least twice improvement in the radio frequency performance of the embedded gate devices. Systematic studies of the radio frequency performance from room temperature down to 20 K are carried out for the first time. A record high extrinsic f_{max} of 17 and 31 GHz for the device with 400 nm gate length has been achieved at room temperature and 20 K, respectively. The ratio of f_{max}/f_T has been improved to over two, a twice improvement over previous results, showing a significant advantage in power gains compared with graphene transistors.[23,24]

2. Results and Discussion

Top-gate BP FETs using a conventional process were designed and fabricated as shown in **Figure 1**a,b. The back-gate dielectric HfO_2 was deposited at 250 °C by ALD with

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The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/aelm.201800138.

DOI: 10.1002/aelm.201800138

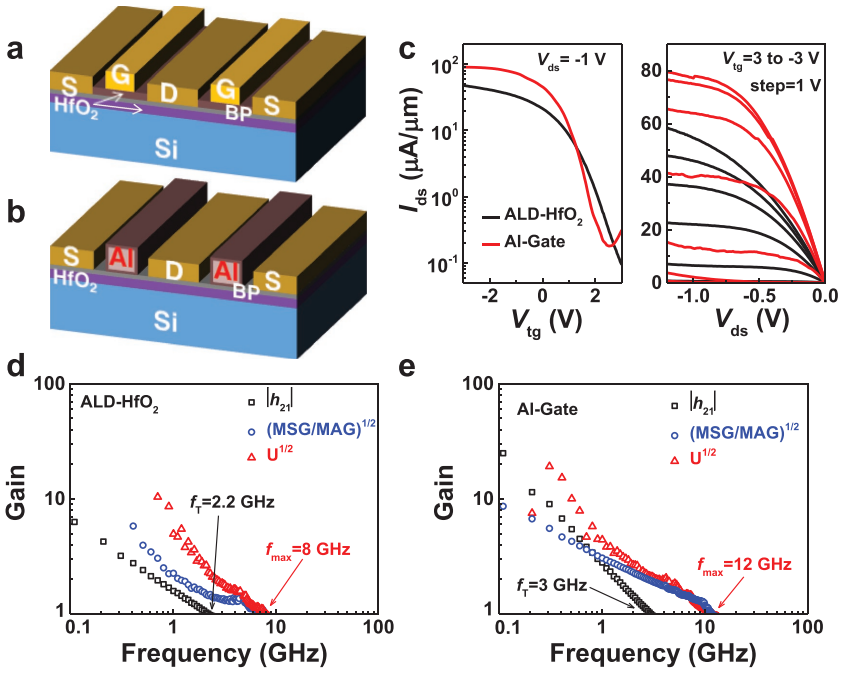

Figure 1. Top-gate device performance. A 3D image of a) ALD-HfO_2 and b) Al-gate top-gate device. c) The transfer and output characteristics of two top-gate devices with gate length of 200 nm at 300 K. Black line: ALD-HfO_2 device; red line: Al-gate device. Small-signal current gain $|h_{21}|$, maximum stable gain (MSG)/maximum available gain (MAG), and Mason's unilateral power gain (U) as a function of frequency for d) ALD-HfO_2 and e) Al-gate top-gate device at 300 K.

tetrakis(ethylmethylamino)hafnium (TEMAHf) and ozone as precursors, followed by rapid thermal annealing (RTA) at 500 °C for 30 s in a nitrogen ambient to improve the dielectric film quality. After the BP flakes were exfoliated and transferred onto the substrate, a stack of 20/60 nm Ni/Au was deposited as source/drain contacts via electron beam lithography (EBL) and electron beam evaporation (EBE). Then, we adopted two approaches for the critical processing step of the top gate. The first approach is the most commonly used top-gate configurations, including ALD high-κ dielectric and the gate electrode, as shown in Figure 1a. The top-gate dielectric HfO_2 was deposited at low temperature (90 °C) using TEMAHf and water as precursors to minimize the thermal budget of BP crystal. In the second approach, 100 nm Al was deposited directly on the BP channel to form the gate without exposure to oxygen precursors. A few nanometer thin oxide of AlO_x around the entire electrode was formed by native oxidation of Al, as shown in Figure 1b. The purpose of a dual-finger gate design is to reduce device resistance and minimize the parasitic effects in the high-frequency operation.[25]

Figure 1c shows the transfer and output characteristics of two representative top-gate devices. The black and red curves represent the direct current (DC) IV properties of the ALD-HfO_2 top-gate and Al-gate device, respectively. Both BP FETs show nearly a similar on/off current ratio of $\approx 10^3$ at $V_{ds} = -1$ V, which originates from the identical thickness (≈10 nm) of the two BP flakes (Figure S1a, Supporting Information). The extracted subthreshold swing (SS) for the ALD-HfO_2 top-gate device is 750 mV dec^{-1}, while SS for Al-gate device is 530 mV dec^{-1}, a 30% enhancement. The output characteristics display good current saturation for both devices. After DC characterization, standard scattering (S) parameter measurement was used to characterize the radio frequency characteristics of top-gate BP RF transistors. Small-signal current gain $|h_{21}|$, maximum stable gain (MSG)/maximum available gain (MAG), and Mason's unilateral power gain (U) extracted from the measured S parameters are shown in Figure 1d,e, respectively. The device extrinsic f_T and f_{max} are measured to be 2.2 and 8 GHz for the ALD-HfO_2 top-gate device. Water precursors during HfO_2 deposition can deteriorate the BP channel material by converting BP into P_xO_y compounds and degrade the channel quality. However, natural oxidation of Al electrode can effectively avoid this process. As a result, the Al-gate device has ≈1.5 × improvement in f_T and f_{max} compared to the ALD-HfO_2 top-gate device. The DC and RF performance of these top-gate devices are still limited by the mobility degradation of BP channel, which results from fixed charge and trap states within the low temperature deposited HfO_2 dielectric and natural oxidation layer of AlO_x. Therefore, novel structure design should be adopted to enhance the performance further and explore the intrinsic properties of BP FETs.

A new embedded gate structure has been developed to minimize the oxidation process and improve the interface quality with respect to a top-gate process described earlier. The fabrication process flow of BP RF transistor with embedded gate can be seen from **Figure 2**a. The original 90 nm SiO_2/Si wafer was patterned using EBL and 70 nm SiO_2 trenches were etched using reactive ion etching (RIE). Subsequently, the trenches were filled with 20/50 nm Ni/Au using EBE with precise alignment, a crucial step to ensure a planarized surface without additional process steps such as chemical mechanical polishing. The atomic force microscopy (AFM) height mapping with embedded gate structure is shown in Figure S1b (Supporting Information), indicating minimal roughness over 6 μm × 6 μm size area. High-κ dielectric HfO_2 was then deposited and annealed at high temperature to minimize the fixed charge in the gate dielectric and the interface state density at HfO_2/BP interface. The BP flake was mechanically exfoliated using the standard scotch-tap method and then transferred onto the embedded gate using pick-and-place dry transfer technology.[26,27] Finally, a stack of 20/60 nm Ni/Au source and drain contacts were deposited to complete the device fabrication. A top view scanning electron microscope (SEM) image of the 400 nm gate-length device is shown in the inset of Figure 2b, with a small gate-to-source (L_{gs}) and gate-to-drain (L_{gd}) spacing of around 50 nm, which minimize the gate-to-source/drain overlap capacitance, a crucial factor in high-frequency response.

The transfer characteristics at room temperature of a representative 400 nm BP FET are shown in Figure 2b, with a typical p-type behavior. The on/off current ratio exceeds 2×10^4 and SS value is 240 mV dec^{-1} at $V_{ds} = -1$ V at 300 K, which can be attributed to the stronger gate coupling and better BP/high-κ interface with respect to the top-gate process mentioned above.

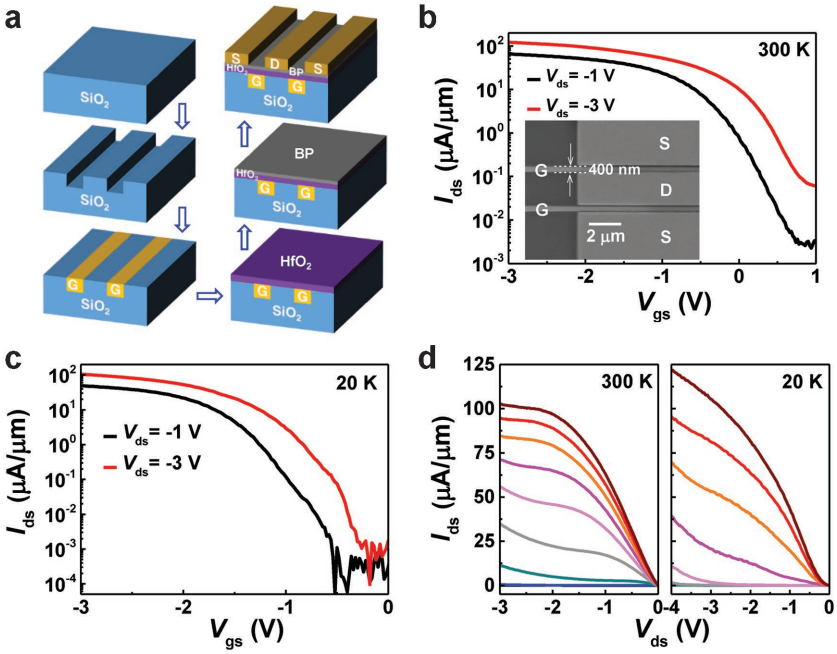

Figure 2. DC characteristics of embedded gate device. a) The fabrication process flow of BP RF transistor with embedded gate. b) The transfer characteristic of the device at 300 K for a 400 nm gate-length device. The inset shows the SEM image of a 400 nm gate-length device. Scale bar: 2 μm. c) The transfer characteristic of the device at 20 K. d) Output characteristics of the same device measured at 300 K (left) and 20 K (right). The drain-to-source voltages sweep from 0 to −3 V at 300 K and from 0 to −4 V at 20 K. The gate-to-source voltages change from 1 to −3 V with a step of −0.5 V, from bottom trace to top trace.

Note here that the BP flake thickness is also about 10 nm as shown in Figure S1a (Supporting Information), so as to make sure that BP flakes thickness are almost the same for a fair comparison with the top-gate devices. The current on/off ratio further increases to 10^5 when the temperature is reduced to 20 K as shown in Figure 2c, originated primarily from the reduction of thermionic carrier density at off-state. The corresponding output characteristics at 300 and 20 K are shown in Figure 2d with decent current saturation properties where a low output conductance defined as $g_0 = dI_{ds}/dV_{ds}$ is critical to improving power gains in RF transistors.[28]

Small-signal current gain ($|h_{21}|$) extracted from the S parameters measured at different drain voltages with L_g = 400 nm at 300 K are shown in **Figure 3**a. An extrinsic peak f_T of 8 GHz before de-embedding is obtained from the frequency at which $|h_{21}|$ rolls off to unity, which is over two times larger than the top-gate devices shown in Figure 1c,d. Previously, DC electronic transport properties have been carried out for BP device at cryogenic temperatures where interesting quantum behaviors can be observed.[6,21,22,29] However, the radio-frequency response of BP RF transistors has been limited at room temperature to date and remained unexplored at low temperatures. In our work, high-frequency measurement is carried out at low temperature, and extrinsic f_T value of 13.5 GHz has been achieved at 20 K as shown in Figure 3b, a significant improvement compared to that at 300 K. Another key figure-of-merit for RF transistor is the maximum oscillation frequency (f_{max}), which is the maximum possible operating frequency at which the power gain becomes unity.[28] An extrinsic f_{max} of 17 GHz has been obtained from a 400 nm device at 300 K as shown in Figure 3c, which is the highest extrinsic f_{max} achieved on BP RF transistor so far and more than twice improvement over the ALD-HfO_2 top-gate device. The value of f_{max} depends much more critically on the output conductance, directly benefiting from the superior current saturation characteristics as indicated in the formula $f_{max} = (f_T/2)/[g_0(R_g+R_s)+2\pi f_T C_{gd} R_g]^{1/2}$, where g_0 is the output conductance, R_g is the gate resistance, R_s is the source resistance, and C_{gd} is the gate to drain capacitance.[30] Furthermore, we measured the high-frequency response at 20 K and record high extrinsic maximum oscillation frequency of 31 GHz has been obtained as shown in Figure 3d. Higher operating frequency can be achieved through

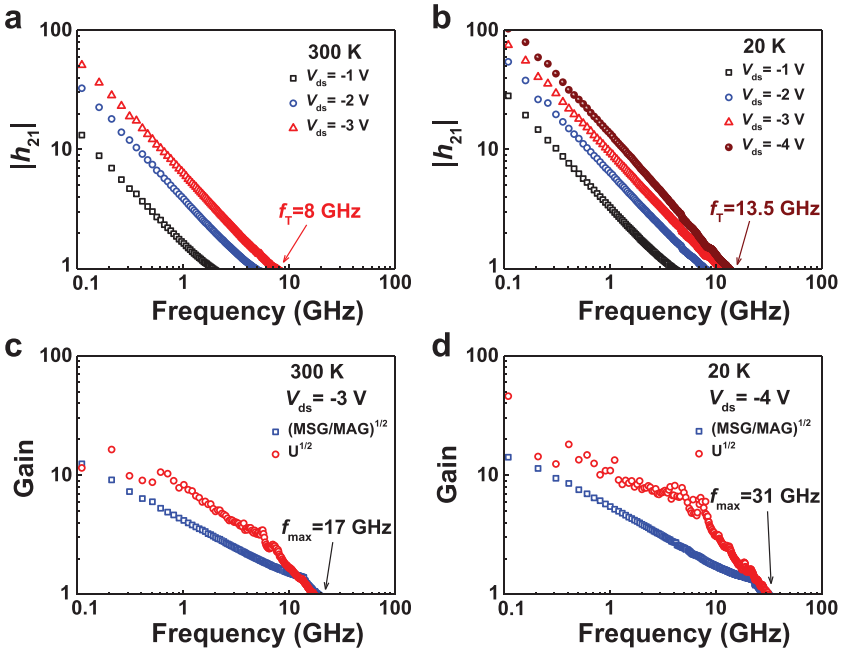

Figure 3. RF performance of the embedded gate device. a) Small-signal current gain $|h_{21}|$ as a function of frequency at 300 K with V_{ds} = −1, −2, and −3 V, respectively. b) $|h_{21}|$ versus frequency at 20 K with V_{ds} = −1, −2, −3, and −4 V, respectively. Measured Mason's unilateral power gain (U), maximum stable gain (MSG), and maximum available gain (MAG) versus frequency for a 400 nm gate-length device at c) 300 K and d) 20 K.

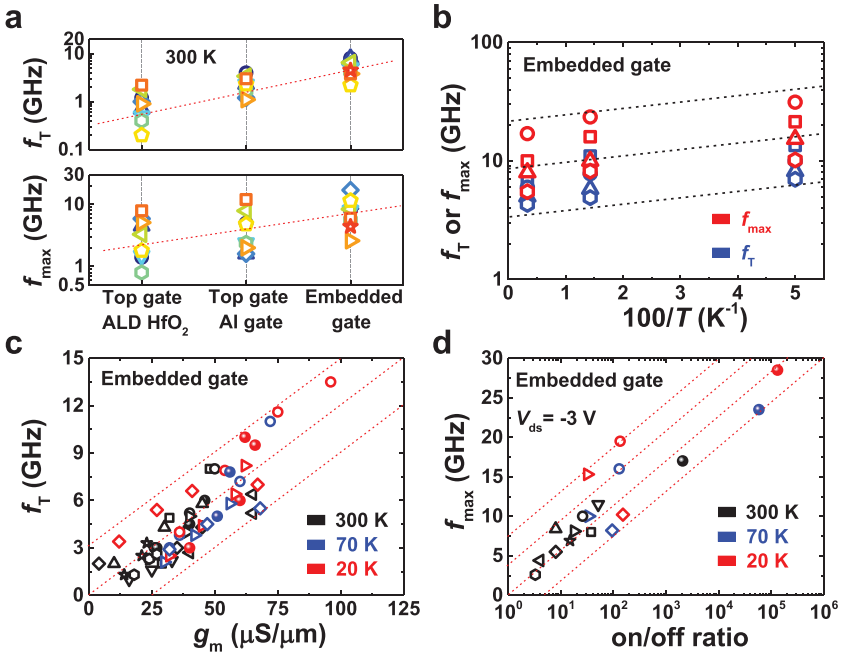

Figure 4. Summary RF performance of the BP FETs. a) The statistics data of extrinsic f_T and f_{max} for three types of devices at 300 K. b) Temperature dependence of the extrinsic peak f_T and f_{max} for four different devices, all show an escalating trend with the temperature decrease. The blue (red) symbol represents the value of f_T (f_{max}). c) f_T versus transconductance for different devices, indicating a statistical distributed linear dependence. The f_T and g_m are extracted at V_{ds} = −1, −2, −3, and −4 V (−4 V only at 20 K), and there has an exact one-to-one correspondence relation between f_T and g_m. d) f_{max} versus current on/off ratio only at V_{ds} = −3 V, showing an approximately linear dependence in the semi-log scale. Black, blue, and red symbol in (c) and (d) represent the values measured at 300, 70, and 20 K, respectively. The gate lengths for all devices range from 200 to 400 nm.

between f_T and g_m. The f_T can be briefly expressed as $f_T = g_m/(2\pi W L_g C_{ox})$, where W is the effective gate width, L_g is the gate length, and C_{ox} is the oxide capacitance.[28] A statistically distributed linear dependence can be clearly observed, which implies performance consistency of the devices. The measured extrinsic f_{max} at V_{ds} = −3 V as a function of the on/off ratio is shown in Figure 4d. Despite the device variation, an increasing trend of the f_{max} and an approximately linear dependence of the on/off ratio in the semi-log scale plot can be observed. This is mainly because of large on–off ratios in DC measurement usually result in better current saturation and smaller output conductance in high-frequency measurement.

The excellent extrinsic RF performance of BP FETs motivates us to explore more functional circuits such as frequency mixers, which are the basic building blocks in modern wireless communication systems.[32] Recently, BP FETs have been characterized for active frequency mixing at the megahertz range.[3] In this paper, we present two types of BP FET-based mixers that are operated at gigahertz frequency. The first is a gate-driven active frequency mixer that is achieved through gate mixing of the local oscillator (LO) and RF input signals, as shown in **Figure 5**a. The LO and RF inputs were combined using an external

further miniaturization of gate length, optimization of layout designs, and reduction of parasitic effects.[31]

To further examine the process stability and to evaluate the consistency of the measurement, we fabricated multiple devices with various BP thicknesses, which were measured at different temperatures. **Figure 4**a shows the data distribution of extrinsic f_T and f_{max} for three types of devices at 300 K. The overall RF performance of the embedded gate devices is better than that of the top-gate devices, showing significant advantages of the embedded gate geometry. As shown in the summary plot of Figure 4b, the extrinsic f_T and f_{max} of four different embedded gate devices all show an increasing trend when temperature decreases. This improvement can be attributed to the higher mobility and saturation velocity due to the reduced scattering from both interface traps and surface phonons at low temperature. Figure 4c shows the extracted extrinsic f_T versus g_m for different devices. The f_T and g_m are extracted at V_{ds} = −1, −2, −3, and −4 V (−4 V only at 20 K), and it exhibits a linear relation

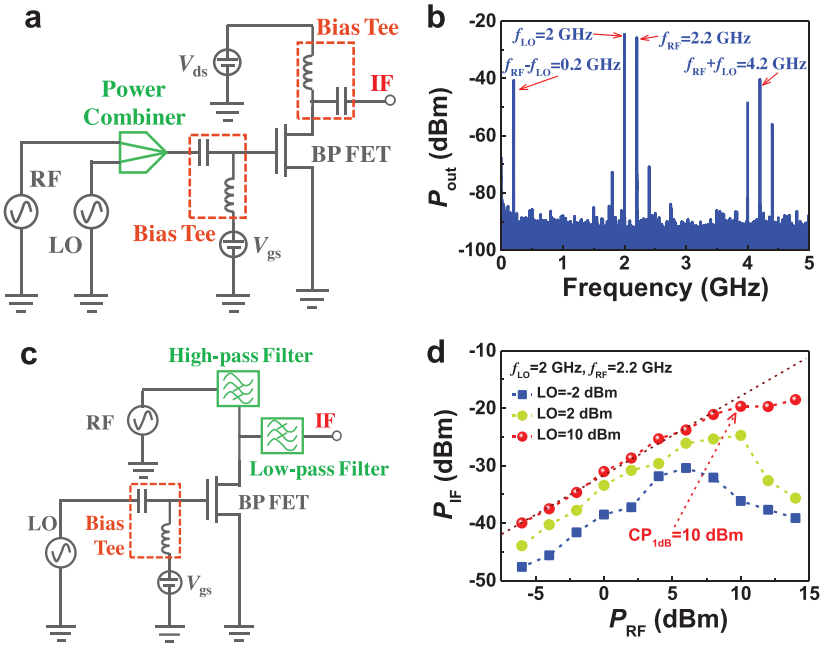

Figure 5. BP FET-based mixer performance. a) Measurement setup for gate-driven active frequency mixer. b) Output frequency spectrum with the input frequency f_{LO} = 2 GHz/f_{RF} = 2.2 GHz and power P_{LO} = P_{RF} = 5 dBm. c) Measurement setup for passive frequency mixer. d) P_{IF} versus P_{RF} at f_{LO} = 2 GHz/f_{RF} = 2.2 GHz for different P_{LO}.

power combiner and then superimposed to the DC gate bias via the bias tee at the gate side. The BP FET mixes them to produce new signals at the sum ($f_{RF} + f_{LO}$) and difference ($f_{RF} - f_{LO}$) frequency of its two input signals. Figure 5b shows the output frequency spectrum with the input frequency f_{LO} = 2 GHz/f_{RF} = 2.2 GHz and power $P_{LO} = P_{RF}$ = 5 dBm. The frequency mixing function can be clearly observed as two dominant peaks at the intermediate frequency (IF) f_{RF}-f_{LO} of 200 MHz and $f_{RF} + f_{LO}$ of 4.2 GHz. In addition, a passive resistive mixer using BP FET has also been demonstrated, which is depicted in Figure 5c. The LO is applied to the gate while the RF is applied to the drain with no drain bias applied, and the desired IF signal is filtered from the drain.[33–35] The measured output power of P_{IF} as a function of P_{RF} with different P_{LO} is shown in Figure 5d, and the P_{IF} increases with high P_{LO}. The mixer linearity is a critical parameter that is usually characterized by the 1 dB compression point (CP_{1dB}).[32] A CP_{1dB} of 10 dBm has been obtained for P_{LO} = 10 dBm, indicating good linearity. Moreover, a decent conversion loss of about 30 dB is achieved with an LO input power P_{LO} of 10 dBm, defined as the power ratio of P_{IF}/P_{RF}.

3. Conclusion

In summary, we have successfully fabricated black phosphorus embedded gate RF transistors using a Damascene-like planarization process with greatly enhanced electrical performance compared to the conventional top-gate structures. Key figures-of-merit such as f_T and f_{max} of multiple devices have been studied systematically at various temperatures down to 20 K for the first time. A record high extrinsic f_{max} of 17 GHz at 300 K has been achieved for a 400 nm gate-length device. Furthermore, an extrinsic f_T of 13.5 GHz and f_{max} of 31 GHz have been obtained at 20 K. Besides, two types of the BP FET-based mixers operating at gigahertz frequency have also been demonstrated. These figures-of-merit indicate the remarkable potential of the BP-based transistors for high-performance, high-frequency applications.

4. Experimental Section

Top-Gate Device: The fabrication process of the top-gate transistors starts with high resistive Si substrate clean using standard RCA-1 solution and diluted hydrofluoric acid (HF). Then, 15 nm thick HfO_2 was deposited as the back-gate dielectric. The depositions were performed at 250 °C using ALD with TEMAHf and ozone as precursors, followed by RTA at 500 °C for 30 s in a nitrogen ambient to improve the dielectric film quality. Few-layer BP flakes were mechanically exfoliated from the purchased natural bulk BP, and then transferred onto the substrate, these processes were performed in a glove box with H_2O and O_2 concentration <1 ppm. In order to minimize the effect of surface degradation, samples with exfoliated BP flakes should be rapidly covered with polymethyl methacrylate (PMMA), and then we look for desired flakes using optical microscopy. Electron beam lithography was used to pattern the source/drain electrodes, and 20/60 nm Ni/Au was deposited by electron beam evaporation to form the source/drain contact. Afterward, we have investigated two methods to perform the critical processing step of top gate. The first method is based on the most commonly used top-gate configurations, including ALD insulating dielectrics and the gate electrode. The top-gate dielectric HfO_2 was deposited at low temperature (90 °C) using TEMAHf and water as precursors. Another method is proposed to preserve BP pristine properties. In this case, 100 nm Al was deposited directly on the BP channel to form the gate. A thin native surface oxidation layer of AlO_x around the entire electrode was formed by natural oxidation of Al.

Embedded Gate Device: Electron beam lithography was used to pattern the gate using photoresist ZEP520 as the mask, and then 70 nm SiO_2 trenches were etched using RIE (CHF_3). Subsequently, very dilute HF was used to smooth the surface of trenches. Next, the trenches were precisely aligned and then filled with 20 nm Ni/50 nm Au using electron beam evaporation. These steps were followed by atomic layer deposition with high-κ dielectrics. Multilayer BP was first exfoliated using the standard mechanical cleavage method from a bulk BP crystal and then transferred onto the embedded gate in the atmospheric environment using a standard dry transfer process. At last, a stack of 20 nm Ni/60 nm Au source and drain contacts were deposited to complete the device. All measurements were performed using LakeShore cryogenic probing system, which enables vacuum and cryogenic measuring environment. *S* parameters were measured up to a frequency of 40 GHz using an Agilent parameter analyzer B1500A, and an N5225A network analyzer. System calibration was carried out at each temperature to ensure the accuracy across the entire temperature range.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

The authors thank He Zhang, Xiangjie Zhao, Ge Gao, and Wei Xu at the Center of Micro-Fabrication and Characterization of Wuhan National Laboratory for Optoelectronics for the support in electron beam lithography and metal deposition. This project was supported by the Natural Science Foundation of China (Grant Nos. 61574066 and 61390504) and the Fundamental Research Funds for the Central Universities (Grant No. 2018KFYYXJJ069).

Conflict of Interest

The authors declare no conflict of interest.

Keywords

black phosphorus, cryogenic temperatures, mixer, radio frequency

Received: March 5, 2018
Revised: April 17, 2018
Published online:

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