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# State-of-the-Art Graphene High-Frequency Electronics

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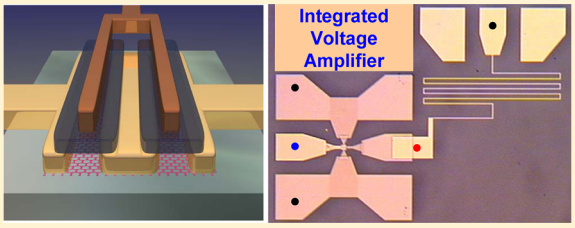
Supporting Information

**ABSTRACT:** High-performance graphene transistors for radio frequency applications have received much attention and significant progress has been achieved. However, devices based on large-area synthetic graphene, which have direct technological relevance, are still typically outperformed by those based on mechanically exfoliated graphene. Here, we report devices with intrinsic cutoff frequency above 300 GHz, based on both wafer-scale CVD grown graphene and epitaxial graphene on SiC, thus surpassing previous records on any graphene material. We also demonstrate devices with optimized architecture exhibiting voltage and power gains reaching 20 dB and a wafer-scale integrated graphene amplifier circuit with voltage amplification.




**KEYWORDS:** *Large-area graphene, radio frequency, voltage gain, power gain, integrated circuit, amplifier*

Graphene possesses great potential for radio frequency (RF) applications such as amplifiers and frequency mixers, whose performance can greatly benefit from the high carrier velocity of graphene.[1−6] Ultrahigh carrier mobility has been demonstrated in mechanically exfoliated flakes under conditions (e.g., suspended graphene at low temperatures) that minimize external perturbations.[7,8] However, technologically relevant graphene devices require large-area synthesized graphene[1−4] supported on and in contact with a substrate, that is, under conditions where the graphene channels are inevitably affected by extrinsic perturbations. With large-area graphene becoming available by either CVD or epitaxial methods,[9,10] it is of great importance to build devices from such technologically relevant graphene materials and to evaluate their performance on high-quality substrates like diamond-like carbon (DLC) and silicon carbide (SiC). Here, we demonstrate and discuss RF field-effect transistors (FET) fabricated on wafer-scale CVD and epitaxial graphene, both achieving record cutoff frequencies surpassing 300 GHz at a scaled channel length of 40 nm. We also conduct a systematic study on the voltage gain and power gain of these graphene transistors and demonstrate significant performance enhancements through improvements in graphene quality, choice of dielectric materials, and the optimal doping of the graphene channel. Finally, we demonstrate a wafer-scale graphene-based, amplifying integrated circuit, with a gain over 3 dB.

**Optimizing Devices on CVD and Epitaxial Graphene.** The interfaces between graphene and its substrate, and between graphene and its top-gate dielectric insulator, are two dominant sources of scattering in graphene devices. Because of the two-dimensional nature of graphene, scattering at these interfaces can lead to a significant degradation of electrical transport and of the resulting device characteristics. Practical solutions to achieving high quality interfaces must be adopted to maintain high transistor performance. For example, commonly used $SiO_2$ substrates introduce scattering associated with trap charges and low-energy surface phonons (59 meV), resulting in deterioration of device performance and of performance uniformity across the wafer. We have previously shown that these effects can be mitigated by using DLC films as substrates, which are advantageous because of the high phonon energy in $sp^3$-hybridized carbon (165 meV) and its nonpolar and the nonhydrophilic nature.[11] Another desirable substrate is silicon carbide, which also possesses a high intrinsic phonon energy (116 meV), and high quality graphene sheets can be directly grown on its surface by epitaxy.[1,2] CVD graphene grown on Cu films and epitaxial graphene grown on SiC are among the two most practical methods of growing large area graphene.[9,10] In this study, we demonstrate and investigate graphene devices fabricated by both approaches.

Single layer graphene is grown on copper foils at temperatures close to 1000 °C while few layer graphene (1−2 layers) is grown epitaxially on semi-insulating SiC substrates at around 1500 °C. The CVD graphene is removed from the copper substrate and then transferred to a DLC substrate. Raman spectroscopy is used to verify the number of layers of the graphene film as well as their doping level. Arrays of graphene RF transistors on both types of graphene materials are then fabricated using the conventional top-down approach. A schematic view of the graphene RF transistor with a dual-channel configuration is shown in Figure 1a. E-beam lithography is employed to define the channel, source and drain contacts, and the gate electrodes. Oxygen plasma etching

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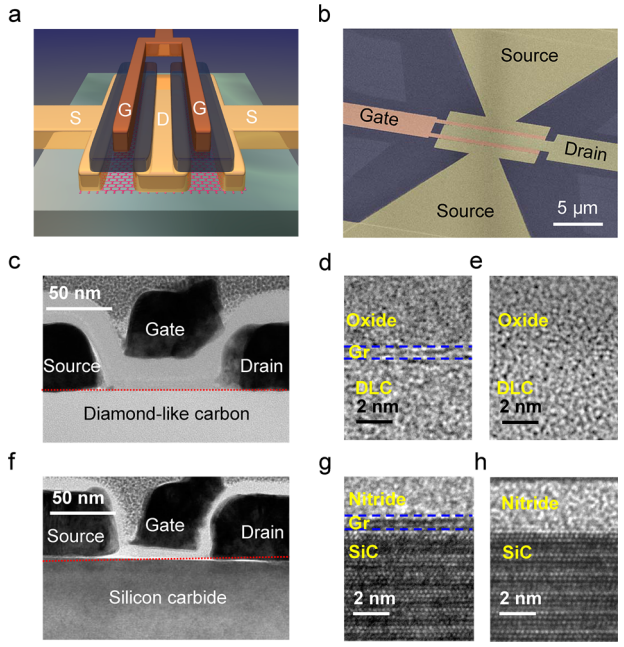


**Figure 1.** Schematic and electron images of graphene RF transistors. (a) Schematic view of a top-gated graphene RF transistor on a DLC substrate (b) SEM image of a typical top-gated dual-channel RF device. The scale bar is 5 $\mu$m. (c) Cross-section TEM images of a transistor based on CVD graphene on DLC; (d,e) the high-resolution TEM image of the channel region of an active device and an open device where graphene is etched away, respectively. (f) Cross-section TEM images of a transistor based on epitaxial graphene on SiC; (g,h) the high-resolution TEM image of the channel region of an active device and an open device where graphene is etched away, respectively. In (c,f) the scale bar is 50 nm. In (d,e,g,h), the scale bar is 2 nm.

is used to remove graphene outside the channel regions. The source and drain contacts consist of Pd/Au metal stacks.

For CVD graphene on DLC, the top-gate dielectric stack includes an electron-beam evaporated and oxidized Al layer followed by an atomic layer deposited (ALD) film of $Al_2O_3$.[12] For epitaxial graphene, 15 nm silicon nitride was grown by plasma-enhanced CVD (PECVD) at 400 °C.[13] These different dielectric materials are adopted for CVD and epitaxial graphene respectively in order to account for the distinct initial doping of the graphene prepared by different methods. The doping of as-prepared CVD graphene is typically p-type with a doping level that increases in air if no passivation layer is used, while the as-grown epitaxial graphene on SiC is intrinsically n-doped with a carrier concentration of $\sim 10^{12}-10^{13}$ cm$^{-2}$. These high doping levels in as-prepared graphene result in a charge neutrality point in a graphene transistor far away from zero gate voltage, and as a result, opposite types of external doping need to be implemented in order to bring the charge neutrality point of the graphene transistor back to zero bias. The minimized channel doping will greatly improve the transconductance as shown in the Supporting Information and also provide better current saturation.[14] As will be discussed later, the control of the doping level in the graphene channel and the corresponding charge neutrality point are essential for maximizing the voltage and power gain of the graphene FETs. As a result, $Al_2O_3$ was chosen as the gate dielectric for CVD graphene because of its electron doping capability of the graphene channel. Similarly, PECVD silicon nitride was adopted as the gate dielectric for epitaxial graphene because it provides p-type doping to the originally n-doped channel. We note that all fabrication steps, including gate dielectric deposition, involve standard top-down, wafer-compatible approaches that can be readily implemented in high-throughput production.

Figure 1b shows a SEM image of a representative dual-channel graphene RF transistor with a ground−signal−ground (GSG) pad design suitable for RF measurements. The total width of the device is 20 $\mu$m. The transmission electron microscopy (TEM) images in Figure 1c,f are those of short channel devices of CVD graphene on DLC and epitaxial graphene on SiC, respectively, with channel lengths of 40 nm. Nearly perfect alignment with small ungated regions of less than 10 nm is attained in our FETs, which is critical to achieving good device performance and reliable parasitics de-embedding results. High-resolution TEM images in Figure 1d,g show channel regions of actual devices with monolayer CVD graphene on DLC and monolayer epitaxial graphene on SiC, respectively, while Figure 1e,h shows the channel regions of corresponding open devices where graphene has been etched away.

**Current and Power Gain of Graphene Transistors.** High-frequency scattering (S) parameters up to 30 GHz were measured using an Agilent network analyzer E8364C with standard GSG probes (details are given in the Methods section). On-chip "open" and "short" structures with identical device layouts are used to de-embed the effects of parasitic capacitances and resistances in the device.[15,16] The cutoff frequency $f_T$, defined as the frequency at which the short-circuit current gain becomes unity, is one of the most important figures-of-merit for evaluating the performance of RF devices and is routinely used to compare the capabilities of different channel materials. For completeness, $f_T$ is extracted using both the linear extrapolation of the −20 dB/dec plot and Gummel's method.[17,18] While cutoff frequencies are of great importance in determining the intrinsic speed of these devices, for analog applications another valuable figure-of-merit is the maximum oscillation frequency $f_{max}$.[19] This value is typically defined as the frequency at which unilateral gain ($U$) becomes unity.[4] $f_{max}$ is the highest possible operating frequency before a transistor loses its ability to amplify power. Much progress has been achieved in increasing $f_T$ in graphene transistors over the past few years with the highest value of 300 GHz achieved on a mechanically exfoliated graphene sample with a nanowire gate.[5] However, the $f_T$ values obtained from devices based on large-area graphene produced by either CVD growth or epitaxial growth on SiC remain lower than those based on exfoliated flakes.[1−4] Figure 2 shows six panels of short-circuit current gain and unilateral power gain, as a function of frequency derived from $S$ parameter measurements of various devices after de-embedding. Results of CVD-graphene devices are shown in Figure 2a−c and those of epitaxial graphene are displayed in Figure 2d−f. Figure 3a shows the intrinsic short-circuit current gain ($|h_{21}|$) for three devices with channel lengths of 650, 300, and 140 nm, possessing cutoff frequencies of 30, 66, and 120 GHz, respectively. Figure 2b shows the short-circuit current gain for a 40 nm long device achieving a $f_T$ above 300 GHz that is twice that of the $f_T$ record for CVD graphene reported previously.[4] This enhancement is mainly due to the improvement in the graphene material quality, as well as the doping control of the gate dielectric as is explained below. Figure 2c shows Mason's unilateral power gain for these four devices with a record high maximum $f_{max}$ of 44 GHz obtained from a 140


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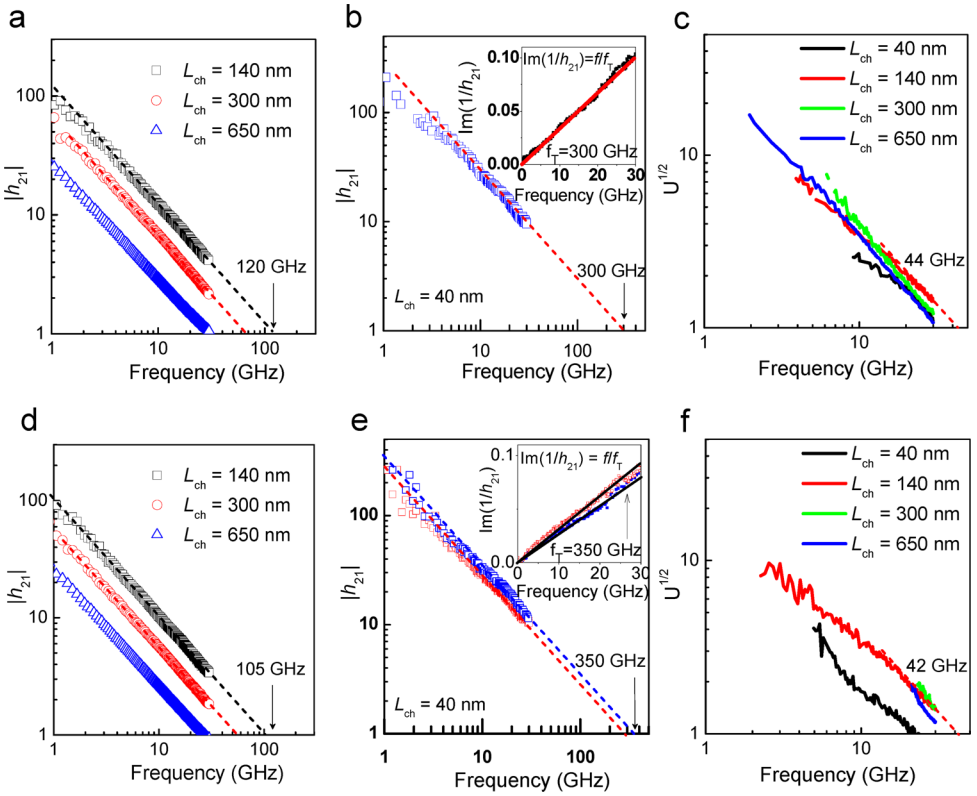


**Figure 2.** RF performance analysis for devices based on CVD graphene and epitaxial graphene. (a–c) These are based on RF devices on CVD graphene on DLC and (d–f) are based on RF devices on epitaxial graphene on SiC. (a) Small-signal current gain $|h_{21}|$ versus frequency for longer channel devices with channel lengths of 140,, 300 and 650 nm. (b) Small-signal current gain $|h_{21}|$ versus frequency for the 40 nm device with a peak $f_T$ of 300 GHz, consistent with the value derived from Gummel's method shown in the inset. (c) Mason's unilateral gain versus frequency for the above four devices, with a peak $f_{max}$ of 44 GHz obtained from the 140 nm device. (d) Small-signal current gain $|h_{21}|$ versus frequency for longer channel devices with channel lengths of 140,, 300, and 650 nm, (e) Small-signal current gain $|h_{21}|$ versus frequency for two 40 nm devices with peak $f_T$ of 300 and 350 GHz, also consistent with the value derived from Gummel's method shown in the inset. (f) Mason's unilateral gain versus frequency for the above four devices with a peak $f_{max}$ of 42 GHz obtained from the 140 nm device.

nm device, which is also a factor of 2 improvement over the previous record of 20 GHz.[4]

The RF performance of epitaxial graphene grown on SiC has been analyzed in a similar fashion, as shown in Figure 2d–f. The peak $f_T$ is also above 300 GHz for 40 nm devices with the highest value of 350 GHz obtained from the best device. This is also supported by the dc projection of $f_T = g_m/2\pi C_{ox}$, where $g_m$ is the transcondutance and $C_{ox}$ is the gate capacitance. Similar to the CVD graphene devices, the peak $f_{max}$ is about 40 GHz for a 140 nm device (see Figure 2f). In Figure 5b, we present the first systematic study of $f_{max}$ in graphene transistors based on large-area synthesized graphene materials. The $f_{max}$ values of 44 and 42 GHz obtained for CVD and epitaxial graphene materials, respectively, are the highest to date for graphene RF devices.

**Voltage Gain for Graphene Transistors.** While $f_T$ and $f_{max}$ are the two most widely used figures-of-merit for evaluating the performance of high frequency transistors for many materials, they present performance limits of devices under special conditions and are thus not sufficient to provide a complete assessment for realistic graphene-based circuits. Specifically, $f_T$ is obtained from the short-circuit current gain $h_{21}$, while the load impedance of any real circuit is nonzero. Also $f_{max}$ describes power gain obtained assuming the best possible impedance matching networks. Open-circuit voltage gain refers to the condition of infinitely high load impedance and thus serves as a more applicable figure-of-merit.[19] This is especially important for graphene-based devices and circuits that exhibit a weak current saturation due to the absence of a bandgap. The open-circuit voltage gain is related to the intrinsic gain, or self-gain, obtained from the transconductance ($g_m$) and the output conductance ($g_d$) as the ratio $g_m/g_d$. Here $g_m$ is the change in the drain current divided by the change in gate voltage at fixed source–drain voltage and $g_d$ is the change in drain current divided by the change in source–drain voltage at fixed gate voltage. In an RF device, the frequency-dependent open-circuit voltage gain can also be derived from *S* parameter measurements as the ac impedance ratio of $z_{21}/z_{11}$ (see Supporting Information for details). At low frequencies, the value of $z_{21}/z_{11}$ should approach the dc intrinsic gain value of $g_m/g_d$. Figure 3a shows the ac voltage gain at a frequency of 200 MHz and the dc intrinsic gain, exhibiting the expected linear relationship, which confirms the value of voltage gain derived from both measurements. Figure 3b shows the voltage gain derived in this way as a function of channel length for RF transistors on both CVD graphene and epitaxial graphene. Voltage gain of more than 20 dB at 1 GHz can be achieved for longer channel devices. This can be explained by the better current saturation behavior with smaller $g_d$ in these devices. This large voltage gain is to our knowledge the highest achieved so far using graphene. The decrease of the voltage gain with decreasing channel length is mainly due to a lack of complete current saturation in short channels. One way of improving the gain is increasing $g_m$ by using a thinner gate dielectric. The


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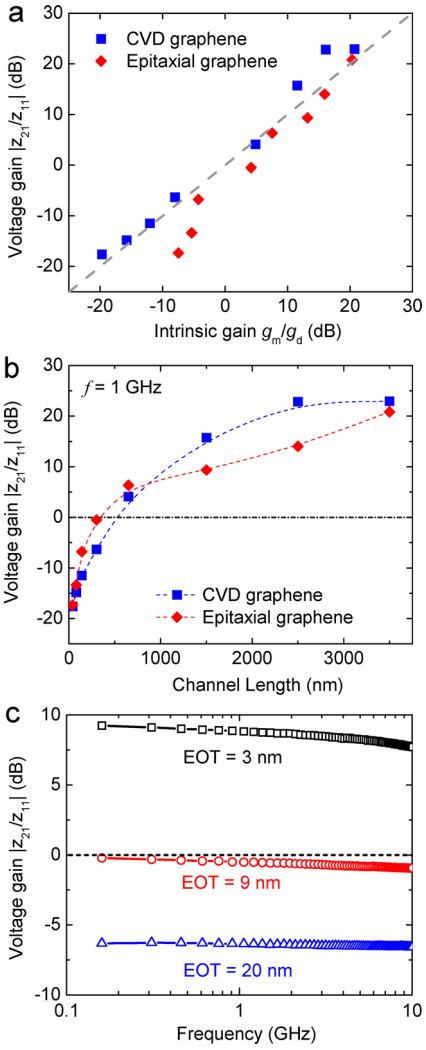


**Figure 3.** Voltage gain analysis for devices based on CVD graphene and epitaxial graphene. (a) Voltage gain of $|z_{21}/z_{11}|$ versus intrinsic gain $g_m/g_d$, showing a linear dependence. The blue square symbols and the red diamond symbols represent CVD graphene and epitaxial graphene, respectively. This shows the uniformity of the graphene devices, consistency of the measurement and accuracy of the de-embedding approach. (b) Voltage gain of $|z_{21}/z_{11}|$ versus channel length at a frequency of 1 GHz. Voltage gain over 20 dB is obtained for long channel devices. (c) Voltage gain of $|z_{21}/z_{11}|$ versus frequency for 300 nm long graphene RF devices with three different EOT values. An improvement of voltage gain of more than 15 dB can be achieved by scaling the EOT from 20 nm down to 3 nm.

resulting larger gate capacitance will not only increase $g_m$, but also help reduce $g_d$ by improving the electro-static gate control. In Figure 3c, we show an improvement in voltage gain of over 15 dB by scaling the EOT from 20 to 3 nm. This illustrates the role of the dielectric thickness and points out a possible way to further improve voltage gain, especially in shorter channel devices.

**Wafer-Scale Graphene Amplifier Integrated Circuit.** Despite the impressive progress achieved on discrete transistors and circuits operating on single graphene devices,[20−23] the barrier of scalable integration of graphene transistors with other elements into a complete circuit remains high. Recently, the fabrication of a graphene integrated mixer circuit (mixer IC) was demonstrated on SiC.[24] A more general use for graphene is as an amplifier. Very recently, the fabrication of an integrated graphene audio amplifier was reported based on exfoliated graphene.[25] A functional amplifier stage must have a voltage gain larger than 0 dB. With the knowledge gained from discrete graphene RF transistors outlined above, we demonstrate here a wafer-scale voltage amplifier circuit where an epitaxial graphene transistor is integrated with a resistive load on a single chip. The common-source circuit layout is shown in Figure 4a, where

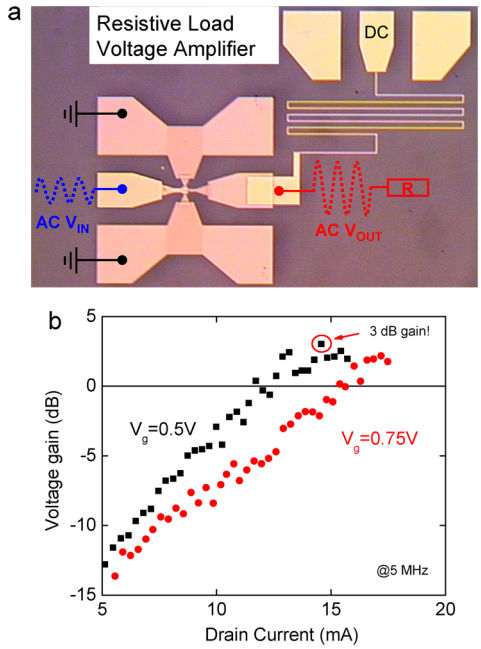


**Figure 4.** Integrated circuit of graphene amplifier on wafer-scale epitaxial graphene on SiC. (a) An optical image of a resistive load integrated circuit. (b) The measured voltage gain versus drain current at 5 MHz for a 1.5 $\mu$m device with a maximum gain of 3 dB.

the high-frequency input signal is applied to the gate electrode and a high-impedance probe applied on the drain electrode is used for monitoring the output voltage. A dc bias applied through the resistive load is used to bias the transistor and a spectrum analyzer is used to measure the output voltage. In order to obtain positive voltage gain for the circuit, the load impedance is chosen to meet the condition $g_m/(g_d + 1/R_{load}) > 1$, As can be seen from Figure 4b, a gain of over 3 dB can be obtained at an operating frequency of 5 MHz.

**Performance Analysis and Outlook.** Figure 5 summarizes the state-of-the-art graphene RF transistors in terms of cutoff frequency and maximum oscillation frequency. Figure 5a shows $f_T$ for both CVD graphene and epitaxial graphene as a function of channel length, exhibiting the typical $1/L$ trend. It is noted that the performance gap between CVD graphene and epitaxial graphene is negligible in our devices. Figure 5b shows $f_{max}$ for both CVD graphene and epitaxial graphene as a function of channel length. Unlike in the case of $f_T$, $f_{max}$ possesses a nonmonotonic behavior when the channel length decreases, and reaches a peak value around 200 nm. This peak in $f_{max}$ is the result of competing contributions from $f_T$, gate resistance, and output conductance $g_d$ as the gate length decreases.[26,27] To further improve the power gain, one needs to improve the saturation behavior of short channel graphene devices, either through gate dielectric down-scaling or through using better graphene material with higher mobility. In this work, the performance gap between graphene and other mature


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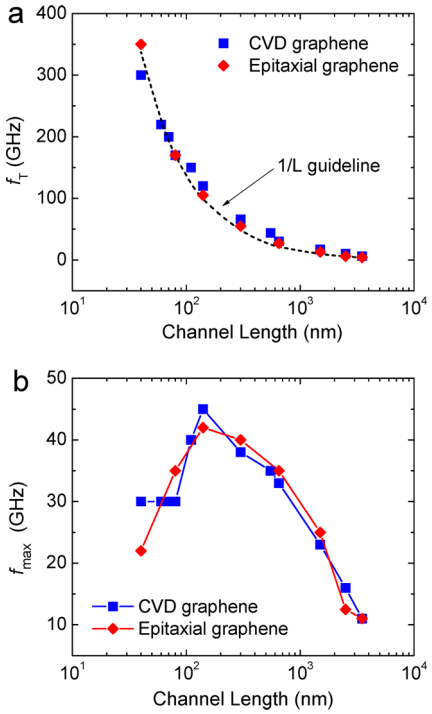


**Figure 5.** Summary of RF performance and benchmarking of graphene devices to other technologies. (a) Scaling behavior of $f_T$ versus channel length, showing the clear $1/L$ dependence. (b) $f_{max}$ versus channel length with the peak $f_{max}$ obtained at a channel length of 140 nm. The blue square symbols and the red diamond symbols represent CVD graphene and epitaxial graphene, respectively.

technologies has been greatly reduced in terms of $f_{max}$.[19] Since $f_{max}$ does not represent the intrinsic performance, but rather is affected mostly by the extrinsic components and layout of the circuit, such as the internal conductance, the gate resistance, capacitance, and feedback, this performance gap can be further reduced through further optimization of these aspects.

**Summary.** Graphene has attracted tremendous research efforts for high frequency applications. However, the excellent performance is usually demonstrated on mechanically exfoliated graphene, which is not suitable for large-scale industrial applications. Moreover, important figures-of-merit such as voltage gain and power gain have rarely been investigated. We have performed systematic studies of high frequency devices fabricated on the large-area graphene materials synthesized by CVD growth on copper and epitaxial graphene grown on SiC. These devices demonstrate drastic performance enhancements for graphene transistors. Detailed analysis of voltage gain and power gain have been carried out with carefully tailored gate dielectric materials for optimal doping in the graphene channel. Using our knowledge of discrete graphene RF devices, an integrated amplifier circuit based on wafer-scale epitaxial graphene exhibiting amplification has also been demonstrated.

**Methods.** CVD grown graphene was grown on copper at 1070 °C in vacuum. After graphene formation, PMMA was spin-coated on top of the graphene layer formed on one side of the Cu foil which then was then dissolved in 1 M iron chloride. The resulting graphene/PMMA layer was then transferred to a desirable substrate (DLC in this case) where the PMMA was later dissolved in acetone. The DLC film was grown on an eight inch Si substrate using cyclohexane ($C_6H_{12}$) in a CVD chamber at 100 mTorr pressure followed by an anneal step at 400 °C for four hours. Epitaxial graphene was grown on the Si face of a semi-insulating 4H silicon carbide wafer. The growth temperature was 1550 °C for 10 min under argon flow. The room temperature carrier mobility was estimated to be around 3000 $cm^2/(V\ s)$ with an n-type density of $10^{12}$ −$10^{13}$ $cm^{-2}$. Metal deposition was done by e-beam evaporation in a vacuum of $10^{-7}$ Torr. A 20 nm Pd/30 nm Au metal stack was used as the source/drain contacts. The gate oxide of $AlO_x$ was formed by an oxidized Al seed layer that was deposited by electron-beam evaporation. This was followed by the deposition of 15 nm $Al_2O_3$ by ALD. A layer of 15 nm $Si_3N_4$ was formed by plasma-enhanced CVD at 400 °C, which served as the gate dielectric for RF devices on epitaxial graphene. In the fabrication of the integrated amplifier circuit, the via through the dielectric was created by etching the $Si_3N_4$ window using $CF_4/O_2$ plasma etching. The resistive load consists of a metal stack of 20 nm Pd and 30 nm Au with a total resistance of about 1200 ohm. The dc and RF characterizations were carried out in a probe station (Lakeshore Inc.) under $<10^{-6}$ Torr using an Agilent parameter analyzer B1500 and network analyzer of E8364C. The system was calibrated using a short-open-load-through (SOLT) method using a standard CS-5 substrate. On-chip open and short structures with exact design layout of the devices were used to de-embed the parasitic effects such as pad capacitance and interconnection resistance.

## ■ ASSOCIATED CONTENT

### Ⓢ Supporting Information

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### Notes

The authors declare no competing financial interest.

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