Performance Optimization of Atomic Layer Deposited ZnO Thin-Film Transistors by Vacuum Annealing

Mengfei Wang, Dan Zhan, Xin Wang, Qianlan Hu, Chengru Gu, Xuefei Li, and Yanqing Wu

***Abstract*— In this letter, high-performance zinc oxide thin-film transistors (ZnO TFTs) have been fabricated on Si substrate by atomic layer deposition (ALD) at 190 °C. The field-effect mobility (μ_{FE}) can be improved from 18.5 $cm^2/V{\cdot}s$ to a record high 43.2 $cm^2/V{\cdot}s$ while maintaining a large I_{on}/I_{off} ratio of 5×10^9 after rapid thermal annealing (RTA) under vacuum at 350 °C. The excellent performance can be attributed to the improvement in the ZnO channel and the interface. The oxygen vacancy ratio in ZnO increases from 36.2% to 40.0%. The interface trap density (N_{it}) between silicon oxide (SiO_2) and ZnO decreases from 5.1×10^{11} $eV^{-1}cm^{-2}$ to 1.4×10^{11} $eV^{-1}cm^{-2}$. Furthermore, the oxide trap density (N_{ot}) of the SiO_2 dielectric reduces from 3.7×10^{19} $eV^{-1}cm^{-3}$ to 1.1×10^{19} $eV^{-1}cm^{-3}$. Finally, we systematically study the electrical performance of the annealed ZnO device at measurement temperature from room temperature of 20 °C to a much higher temperature of 180 °C without device failure.**

***Index Terms*— Atomic layer deposition, ZnO TFTs, interface property, 1/f noise, high temperature.**

I. Introduction

As a wide bandgap semiconductor, zinc oxide (ZnO) has attracted increasing research attention due to its high mobility, high transparency, and low cost for thin-film transistor applications [1]. Large-area and high-quality ZnO layer can be deposited at a low temperature using atomic layer deposition (ALD). Compared with the conventional sputtering method used previous for oxide semiconductors with high mobility [2], [3], the self-limiting surface reaction-based ALD technique could precisely control the thickness, material composition, and doping of the deposited material. It is essential to optimize the electrical performance in both on-state and off-state of the ALD ZnO thin-film transistors (TFTs). Previous work has shown that annealing in hydrogen ambient can increase the on-state current (I_{on}) and mobility of ZnO TFTs. However, this process typically deteriorates the off-state current (I_{off}) and electric stability. On the other hand, annealing in oxygen can improve I_{off} and stability but reduces I_{on} and mobility [4]–[8]. Annealing in nitrogen (N_2) can improve mobility and stability but is less effective in boosting I_{on} due to shallow acceptor doping [4], [9]–[12]. Post-deposition annealing in the air has also been carried out, but it is difficult to accurately optimize the electrical performance due to the complexity of the air composition [13], [14].

In this work, we fabricated ZnO TFTs on Si substrate using ALD growth at 190 °C. Then ALD ZnO TFTs were annealed in vacuum at different temperatures to optimize the electrical performance. The optimized performance can be found at the annealing temperature of 350 °C and the related mechanism was investigated by material characterizations such as x-ray diffraction (XRD) and x-ray photoelectron spectroscopy (XPS), as well as electrical characterization of low-frequency (1/f) noise measurement. Finally, the electrical performance dependence on measurement temperature from 20 to 180 °C has been studied for the 350 °C-annealed devices.

II. Device Fabrication

The top panel of Fig. 1a depicts the cross-section schematic view of ZnO TFT. The substrate consists of a heavily doped p-type silicon (100) layer and a 90 nm thick silicon oxide (SiO_2) dielectric layer. First, the substrate clean was done by the standard RCA process followed by ALD growth of 11 nm thick ZnO at 190 °C. The pulse and purge times of diethylzinc (DEZ) precursor were 0.2 and 6 s, respectively and those of water (H_2O) as an oxygen precursor were 0.2 and 20 s, respectively. Pure N_2 (99.999%) at a flow rate of 300 sccm was used as carrier and purge gases for all precursors. The channel isolation was defined by lithography and then etched with diluted hydrochloric acid. After the definition of source and drain regions by lithography, the substrate was exposed to a mixture of argon and oxygen to remove the residual photoresist and reduce contact resistance. A metal stack composed of 20 nm Ni and 60 nm Au was deposited by e-beam evaporation as the source and drain electrodes. Finally, all the devices were treated by rapid thermal annealing (RTA)

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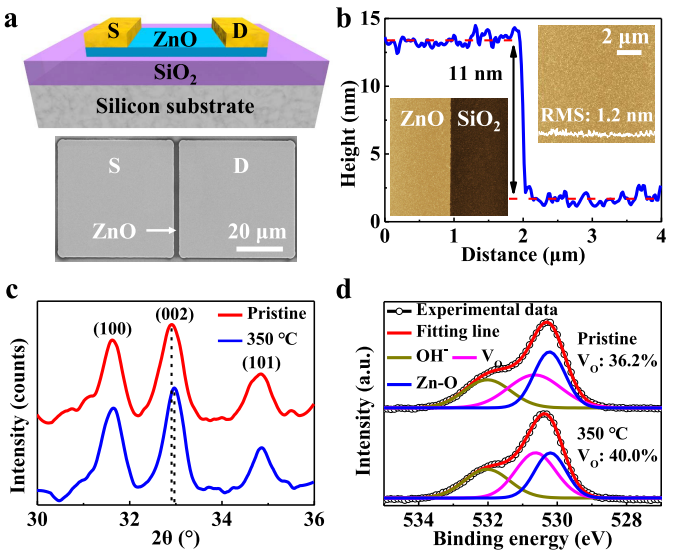

Fig. 1. (a) Top: Cross-section schematic view of the ZnO TFT, bottom: SEM image. Scale bar: 20 μm. (b) AFM images of the device. Scale bar: 2 μm. (c) XRD spectra of pristine and 350 °C-annealed ZnO films. (d) XPS spectra of pristine and 350 °C-annealed ZnO films in the O 1s region.

in vacuum at temperatures varying from 200 to 500 °C for 1 minute.

The lower panel of Fig. 1a shows the scanning electron microscope (SEM) image of the device. The width and length of the channel are 50 μm and 2 μm, respectively. The AFM top-view images of the channel edge and surface are shown in the left and right insets of Fig. 1b, respectively. The thickness and surface roughness root mean square (RMS) of ZnO film is 11 nm and 1.2 nm, respectively. Fig. 1c shows the XRD spectra of pristine and 350 °C-annealed ZnO films in the 2θ range of 30°-36°. The positive shift of the (002) diffraction peak after annealing indicates the optimization of the crystalline quality, including the decrease in lattice constant and the compressive stress release inside the film [4], [10], [15].

Fig. 1d shows the XPS spectra of pristine and 350 °C-annealed ZnO films in the O 1s region. The O 1s peak of each figure can be divided into three peaks by Gaussian fitting with the elimination of a Shirley-type background. The three peaks centered at 530.2 eV, 530.7 eV, and 532 eV, corresponding to O^{2-} ions combined with Zn^{2+} ions, oxygen deficiency like V_O, and chemisorbed oxygen-containing impurities on the channel surface like OH^-, respectively [16], [17]. After vacuum annealing by RTA at 350 °C for 1 minute, the oxygen vacancy ratio of ZnO film rises from 36.2% to 40%.

Electrical measurements were carried out using an Agilent semiconductor analyzer B1500A. The threshold voltage (V_{th}) was extracted by using the standard method of plotting the square root of I_d versus V_g. The maximum drain current (I_{dmax}) was normalized by the channel width and was defined as the I_d at a fixed V_{gt} ($V_{gt} = V_g - V_{th}$) of 10 V and $V_d = 5$ V in transfer characteristics.

III. Result and Discussion

As shown in the transfer and output characteristics in Fig. 2a and 2b, the unannealed device exhibits an I_{on}/I_{off} ratio of

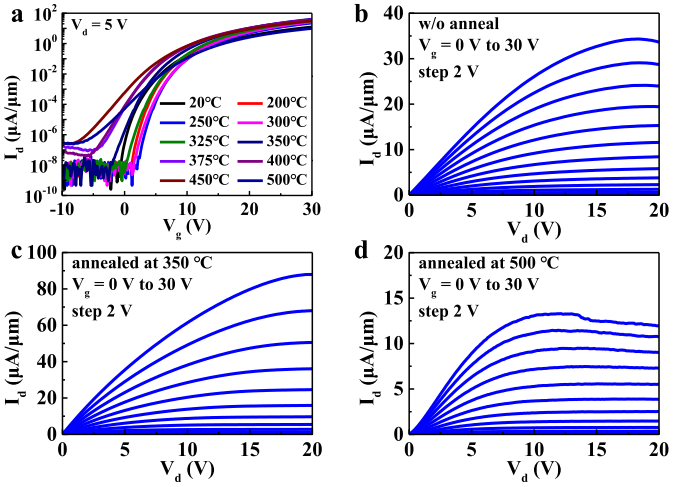

Fig. 2. (a) Transfer characteristics as a function of annealing temperature from 20 to 500 °C. Output characteristics for the device annealed at (b) 20 °C, (c) 350 °C, and (d) 500 °C, respectively.

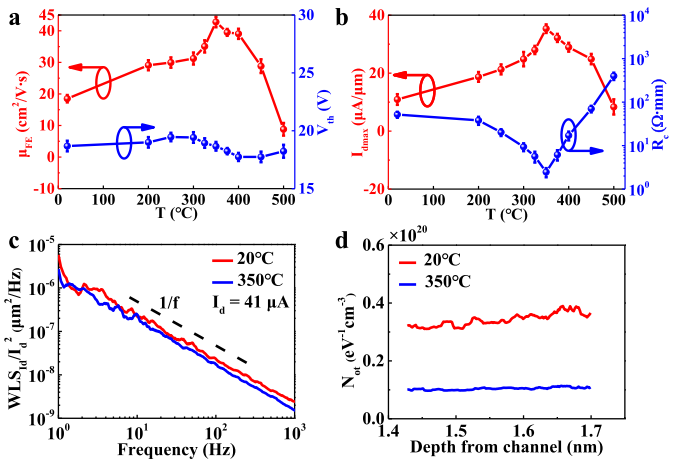

Fig. 3. Dependence of (a) μ_{FE}, V_{th}, (b) I_{dmax}, and R_c on the annealing temperature for 4 devices, respectively. (c) WLS_{Id}/I_d^2 as a function of frequency for unannealed and 350 °C-annealed devices at $I_d = 41$ μA. The ideal 1/f behavior is added for comparison. (d) N_{ot} distribution in the dielectric.

1.9×10^9, a V_{th} of 18.7 V, a μ_{FE} of 18.5 $cm^2/V{\cdot}s$, an I_{dmax} of 10.9 $\mu A/\mu m$, and a contact-resistance (R_c) of 51.8 $\Omega{\cdot}mm$. The output characteristics of the other two key annealing conditions, 350 °C and 500 °C are shown in Fig. 2c and 2d, respectively. Compared to the unannealed device, the I_d of 350 °C-annealed device is significantly increased. However, for the 500 °C-annealed device, the I_d is drastically reduced, and the quality of the interface between the electrode and the channel deteriorates. Also, due to the self-heating effect [18], when V_g is greater than 24 V, the negative differential resistance phenomenon that I_d decreases as V_d increases after reaching the maximum value becomes more obvious.

Fig. 3a and 3d show the dependence of μ_{FE}, V_{th}, I_{dmax}, and R_c on the annealing temperature. As the annealing temperature increases from 20 to 250 °C, the water molecules absorbed on the ZnO surface are gradually removed, resulting in a positive shift in V_{th} and a decrease in SS [19]. When the annealing temperature exceeds 250 °C, the oxygen vacancies start to increase which causes a negative V_{th} shift, while the

TABLE I
SUMMARY OF PREVIOUS WORKS WITH MOBILITY MORE THAN 20 $cm^2/V{\cdot}s$

Ref.	ZnO thickness (nm)	V_{th} (V)	μ_{FE} ($cm^2/V{\cdot}s$)	I_{on}/I_{off}
[22]	45	2.4	20.2	10^5
[6]	50	4.8	21.3	~10^7
[14]	37	4.1	21.9	4×10^8
[23]	20	4.5	27	10^9
[24]	29.4	1.2	27.8	10^9
[25]	14	-1.2	30	10^8
[26]	15	0.1	36.8	~10^7
[27]	16	1.34	37.1	10^7
This work	11	18.7	43.2	5×10^9

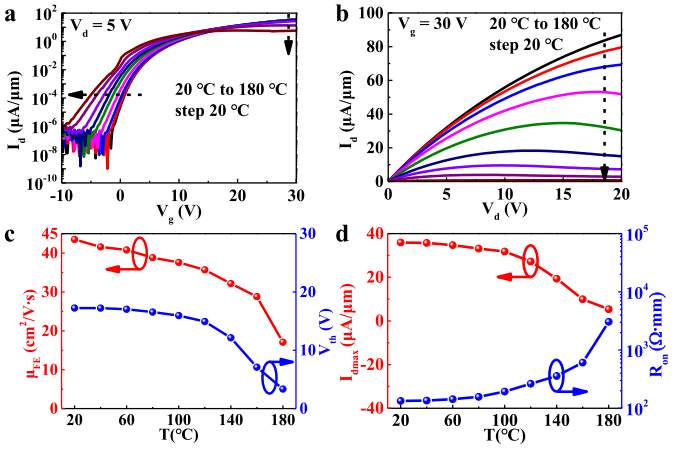

Fig. 4. (a) Transfer characteristics and (b) output characteristics of the 350 °C-annealed device as a function of temperature, respectively. Dependence of (c) μ_{FE}, V_{th}, (d) I_{dmax}, and R_{on} on the temperature, respectively.

decrease in lattice scattering increases μ_{FE} which reaches the highest value at 350 °C. The simultaneous effect of both causes the optimization of I_{dmax} and R_c. At the temperature of 350 °C, the best performance was achieved including an I_{on}/I_{off} ratio of 5×10^9, a μ_{FE} of 43.2 $cm^2/V{\cdot}s$, a V_{th} of 18.7 V, an I_{dmax} of 35.4 $\mu A/\mu m$, and an R_c of 2.5 Ω·mm. When the temperature was further raised from 350 to 500 °C, source and drain contacts deteriorate rapidly due to metal wrinkles, as a result, I_{on}/I_{off} ratio decreases as I_{on} decreases and I_{off} increases, and other characteristics also deteriorate rapidly.

It can be seen from the XRD and XPS that vacuum annealing at 350 °C would affect the ZnO layer by increasing the crystallinity and oxygen vacancies. Here, we performed 1/f noise measurements to investigate the effects of vacuum annealing on SiO_2 and the interface between SiO_2 and ZnO. The measurements were carried out in the linear region with $V_d = 1$ V at 300 K for unannealed and 350 °C-annealed devices.

Fig. 3c shows the normalized noise spectral density (WLS_{Id}/I_d^2) of both devices as a function of frequency at $I_d = 41$ μA. The noise amplitude of the annealed device is lower than that of the unannealed one. The oxide trap density (N_{ot}) distribution in SiO_2 for the two devices was extracted in Fig. 3d according to $N_{ot} = S_{Vg}\alpha f WLC_{ox}^2/kTq^2$, where S_{Vg} is the voltage noise spectral density at $V_g = V_{th}$, α is the tunneling constant and has been set as 10^8 cm^{-1}, C_{ox} is the gate capacitance per unit area, q is the element charge, kT is the thermal energy [20]. The depth (z) of the oxide trap from the channel was derived using $z = -\ln(2\pi f\tau_0)/\alpha$, where τ_0 is the time constant and has been taken as 10^{-10} s. The average N_{ot} of the annealed device is 1.1×10^{19} $eV^{-1}cm^{-3}$, which is 71% lower than that of 3.7×10^{19} $eV^{-1}cm^{-3}$ for the unannealed device.

The interface trap density (N_{it}) was calculated using $N_{it} = S_{Id} f WLC_{ox}^2/g_m^2 kTq^2$, where S_{Id} is the current noise spectral density, g_m is the gate transconductance [21]. The N_{it} of the device after annealing was reduced from 5.1×10^{11} $eV^{-1}cm^{-2}$to 1.4×10^{11} $eV^{-1}cm^{-2}$. These results indicate that the qualities of SiO_2 and interface between SiO_2 and ZnO were improved significantly by vacuum annealing at 350 °C.

Fig. 4a and 4b show the transfer characteristics and output characteristics of the 350 °C-annealed device as a function of measurement temperature. As the measurement temperature increases from 20 to 180 °C with a step of 20 °C, transfer characteristics shift negatively and I_{on}/I_{off} ratio decreases. Also, the μ_{FE}, V_{th}, I_{dmax}, and R_{on} vary monotonically as shown in Fig. 4c and 4d. Due to the increase in oxygen vacancies that produce carriers, the V_{th} shifts negatively as the temperature increases [28]. Also, for the high-purity ZnO channel deposited by ALD, lattice phonon scattering dominates the scattering. Lattice scattering increases as temperature increases which results in the degradation of μ_{FE}. Correspondingly, I_{dmax} decreases and R_{on} increases gradually. As shown in the summary of previous works in Table I, the μ_{FE} of 43.2 $cm^2/V{\cdot}s$ in this work is the highest among ALD ZnO TFTs [6], [14], [22]–[27].

IV. CONCLUSION

We fabricated ZnO TFTs on Si substrate using the ALD technique at 190 °C, and systematically investigated the effect of vacuum annealing on the electrical performance of the devices. The highest μ_{FE} of 43.2 $cm^2/V{\cdot}s$ has been achieved after vacuum annealing at 350 °C for 1 minute. The mechanism of significant performance improvement was investigated in details by XRD, XPS, and 1/f noise measurement. Electrical characteristics of the 350 °C-annealed device at different measurement temperatures varying from 20 to 180 °C have been analyzed. The results of our work show that the electrical performance of ZnO TFTs can be greatly improved by vacuum annealing and can be further optimized with a high-κ dielectric for high-performance display or logic applications.

REFERENCES

[1] E. Fortunato, P. Barquinha, and R. Martins, "Oxide semiconductor thin-film transistors: A review of recent advances," *Adv. Mater.*, vol. 24, no. 22, pp. 2945–2986, May 2012, doi: 10.1002/adma.201103228.

[2] C. W. Shih and A. Chin, "New material transistor with record-high field-effect mobility among wide-band-gap semiconductors," *ACS Appl. Mater. Interfaces*, vol. 8, no. 30, pp. 19187–19191, Jul. 2016, doi: 10.1021/acsami.6b04332.

[3] C. W. Shih, A. Chin, C. Lu, and S. H. Yi, "Extremely high mobility ultra-thin metal-oxide with ns^2np^2 configuration," in *IEDM Tech. Dig.*, Feb. 2015, pp. 6.6.1–6.6.4, doi: 10.1109/IEDM.2015.7409642.

[4] Y. Kawamura, M. Horita, and Y. Uraoka, "Effect of post-thermal annealing of thin-film transistors with ZnO channel layer fabricated by atomic layer deposition," *Jpn. J. Appl. Phys.*, vol. 49, no. 4, Apr. 2010, Art. no. 04DF19, doi: 10.1143/jjap.49.04df19.

[5] J. Yang, J. K. Park, S. Kim, W. Choi, S. Lee, and H. Kim, "Atomic-layer-deposited ZnO thin-film transistors with various gate dielectrics," *Phys. Status Solidi A*, vol. 209, no. 10, pp. 2087–2090, Jul. 2012, doi: 10.1002/pssa.201228303.

[6] Y. Geng, W. Yang, H.-L. Lu, Y. Zhang, Q.-Q. Sun, P. Zhou, P.-F. Wang, S.-J. Ding, and D. W. Zhang, "Mobility enhancement and OFF current suppression in atomic-layer-deposited ZnO thin-film transistors by post annealing in O_2," *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1266–1268, Dec. 2014, doi: 10.1109/LED.2014.2365194.

[7] H. Li, D. Han, L. Liu, J. Dong, G. Cui, S. Zhang, X. Zhang, and Y. Wang, "Bi-layer channel AZO/ZnO thin film transistors fabricated by atomic layer deposition technique," *Nanosc. Res. Lett.*, vol. 12, no. 1, p. 223, Mar. 2017, doi: 10.1186/s11671-017-1999-7.

[8] H.-S. Bae and S. Im, "ZnO-based thin-film transistors of optimal device performance," *J. Vac. Sci. Technol. B, Microelectron.*, vol. 22, no. 3, pp. 1191–1195, May 2004, doi: 10.1116/1.1756166.

[9] K. Remashan, D.-K. Hwang, S.-J. Park, and J.-H. Jang, "Effect of rapid thermal annealing on the electrical characteristics of ZnO thin-film transistors," *Jpn. J. Appl. Phys.*, vol. 47, no. 4, pp. 2848–2853, Apr. 2008, doi: 10.1143/jjap.47.2848.

[10] J.-S. Park, "The annealing effect on properties of ZnO thin film transistors with Ti/Pt source-drain contact," *J. Electroceram.*, vol. 25, nos. 2–4, pp. 145–149, Oct. 2010, doi: 10.1007/s10832-010-9605-8.

[11] Y. W. Jang, S. Bang, H. Jeon, and J. Y. Lee, "Role of postannealing temperature on the microstructure of Al_2O_3/ZnO thin films grown by atomic layer deposition for TFT applications," *Phys. Status Solidi A*, vol. 207, no. 9, pp. 2185–2189, Jun. 2010, doi: 10.1002/pssa.201026065.

[12] J. Zhang, X. F. Li, J. G. Lu, P. Wu, J. Huang, Q. Wang, B. Lu, Y. Z. Zhang, B. H. Zhao, and Z. Z. Ye, "Evolution of electrical performance of ZnO-based thin-film transistors by low temperature annealing," *AIP Adv.*, vol. 2, no. 2, Jun. 2012, Art. no. 022118, doi: 10.1063/1.4711046.

[13] P. Gogoi, R. Saikia, D. Saikia, R. P. Dutta, and S. Changmai, "ZnO TFTs prepared by chemical bath deposition technique with high-k La_2O_3 gate dielectric annealed in ambient atmosphere," *Phys. Status Solidi A*, vol. 212, no. 4, pp. 826–830, Jan. 2015, doi: 10.1002/pssa.201431605.

[14] Y.-H. Wang, Q. Ma, L.-L. Zheng, W.-J. Liu, S.-J. Ding, H.-L. Lu, and D. W. Zhang, "Performance improvement of atomic layer-deposited ZnO/Al_2O_3 Thin-film transistors by low-temperature annealing in air," *IEEE Trans. Electron Devices*, vol. 63, no. 5, pp. 1893–1898, May 2016, doi: 10.1109/TED.2016.2540679.

[15] C. H. Ahn, D. K. Seo, C. H. Woo, and H. K. Cho, "Influence of the thermal annealing temperature of the channel layers grown at room temperature on the device performance in the ZnO thin-film-transistors," *Phys. B, Condens. Matter*, vol. 404, nos. 23–24, pp. 4835–4838, Dec. 2009, doi: 10.1016/j.physb.2009.08.171.

[16] P.-T. Hsieh, Y.-C. Chen, K.-S. Kao, and C.-M. Wang, "Luminescence mechanism of ZnO thin film investigated by XPS measurement," *Appl. Phys. A, Solids Surf.*, vol. 90, no. 2, pp. 317–321, Nov. 2007, doi: 10.1007/s00339-007-4275-3.

[17] A. Abliz, J. Wang, L. Xu, D. Wan, L. Liao, C. Ye, C. Liu, C. Jiang, H. Chen, and T. Guo, "Boost up the electrical performance of InGaZnO thin film transistors by inserting an ultrathin InGaZnO:H layer," *Appl. Phys. Lett.*, vol. 108, no. 21, May 2016, Art. no. 213501, doi: 10.1063/1.4952445.

[18] X. Li, L. Yang, M. Si, S. Li, M. Huang, P. Ye, and Y. Wu, "Performance potential and limit of MoS_2 transistors," *Adv. Mater.*, vol. 27, no. 9, pp. 1547–1552, Mar. 2015, doi: 10.1002/adma.201405068.

[19] J.-S. Park, J. K. Jeong, H.-J. Chung, Y.-G. Mo, and H. D. Kim, "Electronic transport properties of amorphous indium-gallium-zinc oxide semiconductor upon exposure to water," *Appl. Phys. Lett.*, vol. 92, no. 7, Feb. 2008, Art. no. 072104, doi: 10.1063/1.2838380.

[20] X. Li, X. Xiong, T. Li, S. Li, Z. Zhang, and Y. Wu, "Effect of dielectric interface on the performance of MoS_2 transistors," *ACS Appl. Mater. Interfaces*, vol. 9, no. 51, pp. 44602–44608, Dec. 2017, doi: 10.1021/acsami.7b14031.

[21] J. Na, M.-K. Joo, M. Shin, J. Huh, J.-S. Kim, M. Piao, J.-E. Jin, H.-K. Jang, H. J. Choi, J. H. Shim, and G.-T. Kim, "Low-frequency noise in multilayer MoS_2 field-effect transistors: The effect of high-k passivation," *Nanoscale*, vol. 6, no. 1, pp. 433–441, Oct. 2014, doi: 10.1039/C3NR04218A.

[22] Y.-Y. Lin, C.-C. Hsu, M.-H. Tseng, J.-J. Shyue, and F.-Y. Tsai, "Stable and high-performance flexible ZnO thin-film transistors by atomic layer deposition," *ACS Appl. Mater. Interfaces*, vol. 7, no. 40, pp. 22610–22617, Oct. 2015, doi: 10.1021/acsami.5b07278.

[23] D. A. Mourey, D. A. Zhao, J. Sun, and T. N. Jackson, "Fast PEALD ZnO thin-film transistor circuits," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 530–534, Feb. 2010, doi: 10.1109/TED.2009.2037178.

[24] C. H. Ahn, K. Senthil, H. K. Cho, and S. Y. Lee, "Artificial semiconductor/insulator superlattice channel structure for high-performance oxide thin-film transistors," *Sci. Rep.*, vol. 3, no. 1, p. 2737, Sep. 2013, doi: 10.1038/srep02737.

[25] A. Rezk and I. Saadat, "High-performance ALD Al-doped ZnO thin-film transistors grown on flexible substrates," *IEEE Electron Device Lett.*, vol. 40, no. 2, pp. 240–242, Feb. 2019, doi: 10.1109/LED.2019.2890831.

[26] J. Yang, Y. Zhang, Q. Wu, C. Dussarrat, J. Qi, W. Zhu, X. Ding, and J. Zhang, "High-performance 1-V ZnO thin-film transistors with ultrathin, ALD-processed ZrO_2 gate dielectric," *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3382–3386, Aug. 2019, doi: 10.1109/TED.2019.2924135.

[27] X. Chen, G. Zhang, J. Wan, T. Guo, L. Li, Y. Yang, H. Wu, and C. Liu, "Transparent and flexible thin-film transistors with high performance prepared at ultralow temperatures by atomic layer deposition," *Adv. Electron. Mater.*, vol. 5, no. 2, Feb. 2019, Art. no. 1800583, doi: 10.1002/aelm.201800583.

[28] P. K. Nayak, Z. Wang, and H. N. Alshareef, "Indium-free fully transparent electronics deposited entirely by atomic layer deposition," *Adv. Mater.*, vol. 28, no. 35, pp. 7736–7744, Sep. 2016, doi: 10.1002/adma.201600503.