Improved Interface Properties and Dielectric Breakdown in Recessed AlGaN/GaN MOS-HEMTs Using $HfSiO_x$ as Gate Dielectric

Sichao Li, Qianlan Hu, Xin Wang, Tiaoyang Li, Xuefei Li, and Yanqing Wu

***Abstract*— In this letter, we report optimized transport properties in gate recessed enhancement-mode GaN MOS-HEMTs by incorporating silicon into atomic layer deposited gate dielectric HfO_2. Compared with commonly used HfO_2 gate dielectric, the interface trap density can be reduced by nearly an order of magnitude and the fixed oxide traps inside are reduced to almost half using the high-quality passivation of $HfSiO_x$. The MOS-HEMTs based on $HfSiO_x$ exhibit a threshold voltage of 1.5 V, excellent subthreshold swing of 65 mV/dec, and a high on–off ratio of 3×10^{10}. The incorporation of silicon in HfO_2 can also increase the dielectric breakdown property with maximum gate electric field of 2.85 MV/cm for a 10-year time-dependent gate dielectric breakdown lifetime, which is 36% higher than pure HfO_2. The maximum breakdown voltage of $HfSiO_x$ MOS-HEMT is 742 V, which is 30% higher than HfO_2 MOS-HEMT.**

***Index Terms*— Atomic layer deposition, dielectric breakdown, GaN MOS-HEMT, recess gate, interface trap density.**

I. Introduction

NORMALLY-OFF GaN HEMTs are essential for power conversion to maintain system safety and reliability. However, the high density 2DEG at the heterointerfaces keeps the channel normally-on without applying an external electrical field. Typical methods to achieve normally-off HEMTs include fluoride plasma injection, [1], [2], p-type gate [3], [4], partially or fully recessed gate barrier [5]–[7], and a mixture of these mentioned methods [8], [9]. Although threshold voltage can be increased, many of these gate-related modifications will introduce side effects such as high gate leakage and low gate swing. To simplify the gate driver complexity and avoid device failure from gate voltage overshoot, high quality gate dielectrics are necessary not only to suppress gate leakage, but also to maintain 2DEG's inherent high mobility, especially in the case of recess gate structure. Indeed, 2DEG under the recessed area typically suffers from scatterings from poor dielectric/GaN interface, leading to deteriorated gate reliability which poses limits to the commercialization of recessed gate MOS-HEMTs [10], [11].

Numerous dielectrics have been used in recessed gate HEMTs along with various deposition technologies, such as Al_2O_3 [5], [12], MgCaO [13], $LaHfO_x$ [14], SiON [15], SiN_x [6] and multi-layer dielectrics like SiN_x/HfO_2 [16], $SiO_2/LaAlO_3$ [17] and AlN/Al_2O_3 [18]. High-κ gate dielectric HfO_2 stands out among many dielectrics with its high dielectric constant compared with other widely used dielectrics such as SiN_x, SiO_2, Al_2O_3, and AlN. With its higher dielectric constant, HfO_2 MOS-HEMTs can achieve much more efficient electrostatic control. However, HfO_2 on GaN MOS-HEMTs suffers from high leakage current because of insufficient barrier height [19], which will deteriorate device performance via gate leakage. Recent studies have shown the incorporation of silicon into Al_2O_3 can enhance breakdown strength and improve interface properties [20], [21]. In order to improve the dielectric performance of HfO_2, we investigated the inclusion of silicon into HfO_2.

In this letter, we report recessed gate E-mode GaN MOS-HEMTs using silicon doped HfO_2 dielectric and study the effects on device performance from traps between dielectric and channel interface and traps inside dielectrics. $HfSiO_x$ can reduce interface trap density and the fixed oxide traps inside the dielectric, which maintains 2DEG's high mobility property under the recessed gate while achieving normally-off operation. Meanwhile, the incorporation of silicon in HfO_2 can boost the breakdown properties of the dielectric, and thus the breakdown voltage of the device.

II. Device Fabrication

Fig. 1(a) shows the cross-section schematic view of gate recessed GaN MOS-HEMTs. The epitaxial structure consists of a 4 μm buffer layer, a 1 nm AlN insertion layer and a 20 nm $Al_{0.25}Ga_{0.75}N$ barrier layer grown on (111) silicon substrate. The fabrication process started with mesa isolation. Gate recess was performed using low-power Cl_2/BCl_3 plasma etching with an etching depth $\sim$ 20 nm and a smooth etching angle, as shown in Fig. 1(b). Atomic force measurement was used to evaluate the uniformity of the recess surface with a small root mean square roughness of around 0.464 nm. The Ohmic contact regions were deposited with Ti/Al/Ni/Au metal stack, followed by rapid thermal annealing (RTA) at 850° C. Immediately after the HCl dip to remove native oxide, samples were loaded in the atomic

Manuscript received November 29, 2018; accepted December 13, 2018. Date of publication December 19, 2018; date of current version January 31, 2019. This work was supported in part by the China Postdoctoral Science Foundation Funded Project under Grant 2017M622442, in part by the Technology Innovation Project of Hubei Province under Grant 2017AAA127, and in part by the Hubei Province Postdoctoral Scientific and Technological Activities Funded Project under Grant G28. The review of this letter was arranged by Editor D. G. Senesky. *(Corresponding author: Yanqing Wu.)*

The authors are with the Wuhan National High Magnetic Field Center, Huazhong University of Science and Technology, Wuhan 430074, China, and also with the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: yqwu@hust.edu.cn).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2018.2888486

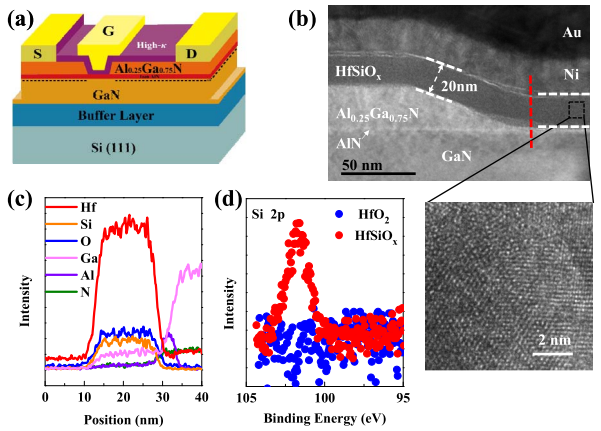

Fig. 1. (a) Cross section schematic of the GaN MOS-HEMT. (b) Cross-sectional TEM image of the recessed GaN MOS-HEMT in the recessed gate area. Inset is the HRTEM of the $HfSiO_x$ dielectric. (c) The EDX analysis of heterointerfaces indicated by the red dashed lined in (b). (d) The XPS spectra in the Si 2p photoemission peak region of the HfO_2 and $HfSiO_x$ surface.

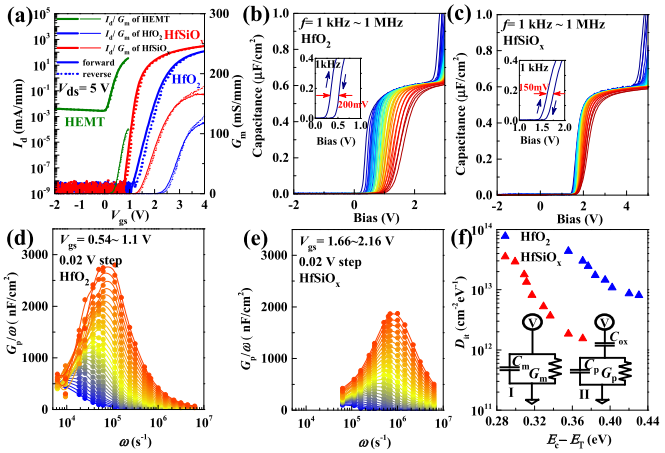

Fig. 2. (a) Double sweep transfer characteristics of HEMTs with 20 nm $HfSiO_x$, with 20 nm HfO_2 and without gate dielectric in saturation region at V_{ds} of 5 V. All HEMTs share the same dimensions: $L_g/L_{gs}/L_{gd}$ = 2/3.5/16 μm. Double sweep CV characteristics of FATFETs (b) with 20 nm HfO_2 and (c) $HfSiO_x$. Frequency dependent conductance as a function of radial frequency for FATFETs (d) with 20 nm HfO_2 and (e) $HfSiO_x$. (f) The interface trap density distribution for FATFETs with HfO_2 and $HfSiO_x$. Inset model (I) is the equivalent circuit model of the FATFET, C_m and G_m are measured capacitance and parallel conductance. Model (II) is the simplified parallel model of the MOS model. The C_{ox} is the oxide capacitance and C_p and G_p are the equivalent parallel capacitance and conductance. All FATFETs share the same dimensions: L_g/W = 100/100 μm.

layer deposition (ALD) chamber for gate dielectric deposition. A 20 nm HfO_2 dielectric was grown using precursors including Tetrakis(dimethylamino)hafnium and ozone at a deposition temperature of 300°C. As for the 20 nm $HfSiO_x$, one cycle reaction of Tris(dimethylamino)silane with ozone was inserted into HfO_2 by after 8 cycles of HfO_2 to form ~1 nm $HfSiO_x$. Devices were completed by Ni/Au gate metal deposition. Besides, the recessed HEMTs without oxide layer were also fabricated using the same process as a control sample. The HRTEM of $HfSiO_x$ in the inset in Fig. 1(b) shows the dielectric is polycrystalline after the final device processing steps. The energy dispersive X-ray (EDX) analysis of the $HfSiO_x$ oxides in Fig. 1(c) confirms Si atoms are uniformly distributed in $HfSiO_x$. Fig. 1(d) depicts the XPS spectra of Si 2p core level from 20 nm HfO_2 or $HfSiO_x$ on recessed GaN epilayer. In the case of $HfSiO_x$, a peak can be discerned at ~102 eV, confirming the Si atoms in the $HfSiO_x$ dielectric, while this peak is absent in HfO_2.

III. Results and Discussion

Fig. 2(a) compares the transfer characteristics of HEMTs in saturation region. The recessed HEMT shows V_{tsat} of 0.75 V and SS of 133 mV/dec. The $g_{m,max}$ of HEMT is 109 mS/mm, which is lower than MOS-HEMT since it is overwhelmed by the gate leakage. The HfO_2MOS-HEMT exhibits increased V_{tsat} of 2.7 V, owing to the leakage blocking capability, but it shows large SS of 129 mV/dec. With the incorporation of silicon in HfO_2, the device performance has been significantly improved with near-ideal SS of 65 mV/dec, indicating lower interface trap density. The V_{tsat} shifts to 1.5 V, which can be attributed to less acceptor-like traps in $HfSiO_x$ compared with HfO_2. Both MOS-HEMTs exhibit a high on/off ratio above 10^{10}. The $HfSiO_x$ MOS-HEMT exhibits negligible hysteresis between forward and reverse sweep, which is smaller than HfO_2MOS-HEMT, indicating the suppression of interface traps.

To further understand the correlation between gate dielectrics and device performance, multi-frequency conductance method was applied to the FATFET structure with L_g/W_g = 100/100 μm following the same device fabrication process as MOS-HEMTs [22], [23]. Fig. 2(b) shows the multi-frequency CV characteristics of HfO_2 FATFET with clockwise hysteresis ~ 200 mV at 1 kHz, which is slightly larger than 150 mV of $HfSiO_x$ FATFET in Fig. 2(c). The frequency dependent V_{fb} for $HfSiO_x$ FATFET is only 0.6 V, which is much smaller than 1.5 V for HfO_2 FATFET. At lower frequencies, the capacitance starts to increase from interface traps response, while at higher frequencies, slow traps cannot respond and the capacitance comes primarily from fast traps, which indicates large amount of slow traps located within HfO_2 or at the HfO_2/III-N interface, compared with $HfSiO_x$.

The gate-to-channel capacitance and conductance were measured with high terminal on the gate and low terminal on the source and drain of the FATFET, as shown in the model I in Fig. 2 (f). The parallel capacitance C_p and conductance G_p can be extracted by subtracting the oxide capacitance, as shown in the model II. And the interface trap density can be extracted by the equation $D_{it} = 2.5(G_p/\omega)_{peak}/q$, where q is the electron charge [23], [24]. The trap energy level is given by $\Delta E = k_B T \ln(N_c \sigma_n \upsilon_t \tau_T)$, where k_B is the Boltzmann constant, T is the temperature, N_c is the effective conduction band DOS, σ_n is the capture cross-section, υ_t is the thermal velocity of electrons, τ_T is the interface trap time constant corresponding with $2/\omega_c$ [23], [24]. Fig. 2(d) shows that G_p/ω peak of HfO_2/III-N interface gradually increases with ω, indicating higher interface trap density for interface traps with shorter emission constant. The G_p/ω peak movement of $HfSiO_x$/III-GaN interface in Fig. 2(e) reveals the same trend, and that the characterized interface traps by conductance method exhibit shorter emission time constant between 1 μs and 10 μs compared with HfO_2/III-N interface. As shown in Fig. 2(f), the minimal D_{it} extracted at E_c-E_t = 0.37 eV is 1.6 × 10^{12} $cm^{-2}eV^{-1}$ at $HfSiO_x$/III-N interface, much lower than the minimal D_{it} of 8.1 × 10^{12} $cm^{-2}eV^{-1}$ of HfO_2/III-GaN interface at E_c-E_t = 0.43 eV. These D_{it} values extracted from conductance method are in accordance with SS obtained from

subthreshold region of I_D-V_{GS} curve, confirming better interface properties for $HfSiO_x$ MOS-HEMT. It is supposed that the acceptor-like traps within the HfO_2 can be suppressed by SiO_2 interlayer [25]. Other works also show the incorporation of SiO_2 into high-κ dielectrics can screen the soft optical phonons associated with the highly polarizable bonds in high-κ dielectric HfO_2 [26].

In the multi-frequency CV measurement, only trap states with characteristic frequencies lying within 1 kHz $\sim$ 1 MHz will contribute the single type interface trap signature during the measurement. Deep level traps within the oxide cannot follow the lowest gate signal frequency. In order to further characterize trap energy level within dielectrics, high-κ/III-N MIS structures were characterized by capacitance-mode deep-level transient spectroscopy. For both MISCAPs, the reverse bias was selected at pinch-off region, and the filling pulse bias was applied in strong inversion to fill the traps within the dielectrics. As shown in Fig. 3(a), one peak was found in HfO_2 MISCAP, indicating one electron trap level in HfO_2. While two lower peaks were observed in $HfSiO_x$, which indicates two electron trap levels. The activation energy and capture cross-section can be obtained from Arrhenius plot based on the equation $\ln(e/T^2) = \ln(16\pi\sigma_n k_B^2 m_n/h^3) - \Delta E_T/k_B T$, where e is the electron emission rate, m_n is the effective electron mass and h is the plank constant [27]. Fig. 3(b) shows the Arrhenius plot, the slope yields an energy level of 0.41 eV in HfO_2, while there exist two shallower trap levels in $HfSiO_x$ at 0.3 eV and 0.07 eV. The capture cross section of the trap in HfO_2 is 1.7×10^{-11} cm^2, while the traps cross sections in $HfSiO_x$ are 4.4×10^{-11} and 2.1×10^{-17} cm^2. The trap concentration N_T can be obtained from $N_T = 2\Delta C/C_0 N_A$, where N_D is the net donor concentration obtained from CV profiling, ΔC is the difference between the capacitance when the traps are filled and emptied, and C_0 is the steady state capacitance [27]. The trap concentration of HfO_2 is 4×10^{12} cm^{-3}, which is almost twice the number in $HfSiO_x$ with trap concentrations of 2.7×10^{12} cm^{-3} and 2.1×10^{12} cm^{-3}. Based on the CV analysis and DLTS analysis, the defects properties in HfO_2 and $HfSiO_x$ are uncovered and compared. As shown in Fig. 3(c), the highly polarizable bonds in high-κ dielectric HfO_2 induces large number of oxide traps as well as interface traps. With the incorporation of SiO_2 into high-κ dielectrics, two shallower trap levels are formed, as shown in Fig. 3(d). The new trap levels can screen the soft optical phonons associated with the polarizable bonds in HfO_2, and mitigate its interaction on dielectric/III-N interface and channel mobility [26].

To evaluate the reliability of these MOS-HEMTs, three groups of devices were stressed at constant gate-source voltage with source and drain grounded for each MOS-HEMT. The time when the current suddenly increases is defined as time-to-breakdown t_{BD}. Fig. 4(a) shows the time-to-breakdown is Weibull distributed for HfO_2 MOS-HEMTs and linear fitting was used for the full range. The Weibull slope of HfO_2 decreases from 4.2 to 1.5 with increasing oxide field. The oxide breakdown can be ascribed to field-induced defects. Under high oxide field, the traps needed to form the conductive breakdown path are randomly redistributed within the oxide and are broad spread statistically, which results in smaller Weibull slope [28]. Fig. 4(b) shows the Weibull slope of $HfSiO_x$ MOS-HEMTs decreases from 3.8 to 2.0 with increased oxide field. The analysis of time-to-breakdown at 63.2% failure

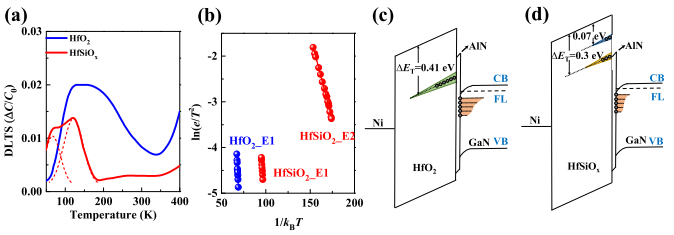

Fig. 3. (a) C-DLTS spectra of recessed GaN MISCAPs with 20 nm $HfSiO_x$ and 20 nm HfO_2 at t_1/t_2 = 2 ms/15 ms. (b) The Arrhenius plot for the deep level traps for both MISCAPs. One electron trap was observed in HfO_2, while two electron traps were observed in $HfSiO_x$. Band diagram of GaN MOS-HEMT devices with (c) 20 nm HfO_2 and (d) 20 nm $HfSiO_x$ at positive gate-source bias.

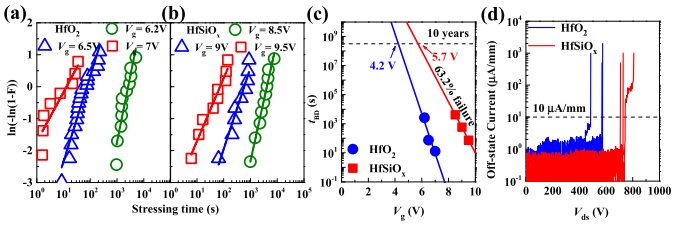

Fig. 4. Weibull distribution of time-to-breakdown for (a) HfO_2 and (b) $HfSiO_x$ MOS-HEMTs. The Weibull slopes of HfO_2 MOS-HEMTs are 4.2, 2.7, and 1.5 for V_G = 6.2 V, 6.5 V and 7 V, respectively. The Weibull slopes of $HfSiO_x$ MOS-HEMTs are 3.8, 2.5, and 2.0 for V_G = 8.5V, 9V and 9.5V, respectively. (c) Lifetime prediction of 63.2% failure level for HfO_2 and $HfSiO_x$ gate dielectrics. (d) Off-state characteristics of several HfO_2 and $HfSiO_x$ MOS-HEMTs with the same dimensions at gate-source bias of 0 V. The dimensions are $L_G/L_{GS}/L_{GD}$ = 2/3.5/16 μm.

rate (i.e. ln(-ln(1-F) = 0) for each dielectric allows one to predict the lifetime, as shown in Fig. 4(c) [29]. The maximum gate bias for ten-year lifetime is extracted to be 5.7 V ($\sim$2.85 MV/cm) for $HfSiO_x$ MOS-HEMT and 4.2 V ($\sim$2.1 MV/cm) for HfO_2 MOS-HEMT at 63% failure level. The better time-to-breakdown of the $HfSiO_x$ MOS-HEMT can be attributed to the better dielectric interface as well as the larger energy band offset of $HfSiO_x$ on III-N compared with HfO_2 which effectively suppress gate leakage current and increase the electric field strength [30]. The reversible breakdown property in ultra-thin dielectrics is not observed in power MOS-HEMTs with thick dielectrics [31].

Fig. 4(d) shows the off-state breakdown voltage for both E-mode MOS-HEMTs. The reduced interface defects and high electric strength of $HfSiO_x$ can enhance the off-state breakdown voltage as well. For HfO_2 MOS-HEMTs, drain-source current starts to increase after a drain-source bias of 400 V, then sharply increase to 10 μA/mm with a maximum drain-source bias $\sim$ 580 V. With suppressed gate leakage current, the off-state current of HfSiOx MOS-HEMT remains below 1 μA/mm up to a drain-source voltage of 700 V, resulting in a much higher off-state breakdown voltage of 742 V.

IV. Conclusion

In conclusion, this letter reports high-κ dielectrics in recessed gate E-mode GaN MOS-HEMTs, and silicon inclusion into HfO_2 dielectric provides better passivation in the recess channel region and minimized interface and fixed oxide traps and near-ideal subthreshold slope can be achieved. The dielectric breakdown strength of the E-mode GaN MOS-HEMTs can also be improved using $HfSiO_x$ as gate dielectric compared to that based on HfO_2.

REFERENCES

[1] K. J. Chen, L. Yuan, M. J. Wang, H. Chen, S. Huang, Q. Zhou, C. Zhou, B. K. Li, and J. N. Wang, "Physics of fluorine plasma ion implantation for GaN normally-off HEMT technology," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 2011, pp. 19.4.1–19.4.4, doi: 10.1109/IEDM.2011.6131585.

[2] X. Sun, Y. Zhang, K. S. Chang-Liao, T. Palacios, and T. P. Ma, "Impacts of fluorine-treatment on E-mode AlGaN/GaN MOS-HEMTs," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2014, pp. 17.3.1–17.3.4, doi: 10.1109/IEDM.2014.7047070.

[3] Y. Uemoto, T. Morita, A. Ikoshi, H. Umeda, H. Matsuo, J. Shimizu, M. Hikita, M. Yanagihara, T. Ueda, T. Tanaka, and D. Ueda, "GaN monolithic inverter IC using normally-off gate injection transistors with planar isolation on Si substrate," in *IEDM Tech. Dig.*, Baltimore, MD, USA, Dec. 2009, pp. 7.6.1–7.6.4, doi: 10.1109/IEDM.2009.5424397.

[4] X. Li, M. Van Hove, M. Zhao, K. Geens, V.-P. Lempinen, J. Sormunen, G. Groeseneken, and S. Decoutere, "200 V enhancement-mode p-GaN HEMTs fabricated on 200 mm GaN-on-SOI with trench isolation for monolithic integration," *IEEE Electron Device Lett.*, vol. 38, no. 7, pp. 918–921, Jul. 2017, doi: 10.1109/LED.2017.2703304.

[5] Q. Zhou, L. Liu, A. Zhang, B. Chen, Y. Jin, Y. Shi, Z. Wang, W. Chen, and B. Zhang, "7.6 V threshold voltage high-performance normally-off Al_2O_3/GaN MOSFET achieved by interface charge engineering," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 165–168, Feb. 2016, doi: 10.1109/LED.2015.2511026.

[6] M. Hua, Z. Zhang, J. Wei, J. Lei, G. Tang, K. Fu, Y. Cai, B. Zhang, and K. J. Chen, "Integration of LPCVD-SiN_x gate dielectric with recessed-gate E-mode GaN MIS-FETs: Toward high performance, high stability and long TDDB lifetime," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2016, pp. 10.4.1–10.4.4, doi: 10.1109/IEDM.2016.7838388.

[7] M. Hua, J. Wei, G. Tang, Z. Zhang, Q. Qian, X. Cai, N. Wang, and K. J. Chen, "Normally-Off LPCVD-SiN_x/GaN MIS-FET with crystalline oxidation interlayer," *IEEE Electron Device Lett.*, vol. 38, no. 7, pp. 929–932, Jul. 2017, doi: 10.1109/LED.2017.2707473.

[8] C. Liu, S. Yang, S. Liu, Z. Tang, H. Wang, Q. Jiang, and K. J. Chen, "Thermally stable enhancement-mode GaN metal-isolator-semiconductor high-electron-mobility transistor with partially recessed fluorine-implanted barrier," *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 318–320, Apr. 2015, doi: 10.1109/LED.2015.2403954.

[9] H. Okita, M. Hikita, A. Nishio, T. Sato, K. Matsunaga, H. Matsuo, M. Tsuda, M. Mannoh, S. Kaneko, M. Kuroda, M. Yanagihara, A. Ikoshi, T. Morita, K. Tanaka, and Y. Uemoto, "Through recess and regrowth gate technology for realizing process stability of GaN-based gate injection transistors," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 1026–1031, Mar. 2017, doi: 10.1109/TED.2017.2653847.

[10] P. Lagger, C. Ostermaier, G. Pobegen, and D. Pogany, "Towards understanding the origin of threshold voltage instability of AlGaN/GaN MIS-HEMTs," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2012, pp. 13.1.1–13.1.4, doi: 10.1109/IEDM.2012.6479033.

[11] T.-Li Wu, J. Franco, D. Marcon, B. De Jaeger, B. Bakeroot, S. Stoffels, M. Van Hove, G. Groeseneken, and S. Decoutere, "Toward understanding positive bias temperature instability in fully recessed-gate GaN MISFETs," *IEEE Trans. Electron Devices*, vol. 63, no. 5, pp. 1853–1860, May 2016, doi: 10.1109/TED.2016.2539341.

[12] S. Huang, Q. Jiang, K. Wei, G. Liu, J. Zhang, X. Wang, Y. Zheng, B. Sun, C. Zhao, H. Liu, Z. Jin, X. Liu, H. Wang, S. Liu, Y. Lu, C. Liu, S. Yang, Z. Tang, J. Zhang, Y. Hao, and K. J. Chen, "High-temperature low-damage gate recess technique and ozone-assisted ALD-grown Al_2O_3 gate dielectric for high-performance normally-off GaN MIS-HEMTs," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2014, pp. 17.4.1–17.4.4, doi: 10.1109/IEDM.2014.7047071.

[13] H. Zhou, X. Lou, S. B. Kim, K. D. Chabak, R. G. Gordon, and P. D. Ye, "Enhancement-mode AlGaN/GaN fin-MOSHEMTs on Si substrate with atomic layer epitaxy MgCaO," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1294–1297, Sep. 2017, doi: 10.1109/LED.2017.2731993.

[14] Y. C. Lin, Y. X. Huang, G. N. Huang, C. H. Wu, J. N. Yao, C. M. Chu, S. Chang, C. C. Hsu, J. H. Lee, K. Kakushima, K. Tsutsui, H. Iwai, and E. Y. Chang, "Enhancement-mode GaN MIS-HEMTs with $LaHfO_x$ gate insulator for power application," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1101–1104, Aug. 2017, doi: 10.1109/LED.2017.2722002.

[15] H.-S. Kim, S.-W. Han, W.-H. Jang, C.-H. Cho, K.-S. Seo, J. Oh, and H.-Y. Cha, "Normally-off GaN-on-Si MISFET using PECVD SiON gate dielectric," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1090–1093, Aug. 2017, doi: 10.1109/LED.2017.2720719.

[16] W. Choi, O. Seok, H. Ryu, H.-Y. Cha, and K.-S. Seo, "High-voltage and low-leakage-current gate recessed normally-off GaN MIS-HEMTs with dual gate insulator employing PEALD-SiN_x/RF-sputtered-HfO_2," *IEEE Electron Device Lett.*, vol. 35, no. 2, pp. 175–177, Feb. 2014, doi: 10.1109/LED.2013.2293579.

[17] C. Y. Tsai, T. L. Wu, and A. Chin, "High-performance GaN MOSFET with high-κ $LaAlO_3/SiO_2$ gate dielectric," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 35–37, Jan. 2012, doi: 10.1109/LED.2011.2172911.

[18] J. Wei, S. Liu, B. Li, X. Tang, Y. Lu, C. Liu, M. Hua, Z. Zhang, G. Tang, and K. J. Chen, "Enhancement-mode GaN double-channel MOS-HEMT with low on-resistance and robust gate recess," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 2015, pp. 9.4.1–9.4.4, doi: 10.1109/IEDM.2015.7409662.

[19] T. E. Cook, Jr., C. C. Fulton, W. J. Mecouch, R. F. Davis, G. Lucovsky, and R. J. Nemanich, "Band offset measurements of the GaN (0001)/HfO_2 interface," *J. Appl. Phys.*, vol. 94, no. 11, pp. 7155–7158, Aug. 2003, doi: 10.1063/1.1625579.

[20] S. H. Chan, M. Tahhan, X. Liu, D. Bisi, C. Gupta, O. Koksaldi, H. Li, T. Mates, S. P. Denbaars, and S. Keller, "Metalorganic chemical vapor deposition and characterization of (Al,Si)O dielectrics for GaN-based devices," *Jpn. J. Appl. Phys.*, vol. 55, no. 2, p. 021501, Jan. 2016, doi: 10.7567/JJAP.55.021501.

[21] S. H. Chan, S. Keller, O. S. Koksaldi, C. Gupta, S. P. Denbaars, and U. K. Mishra, "Exploring metalorganic chemical vapor deposition of Si-alloyed Al_2O_3 dielectrics using disilane," *J. Cryst. Growth*, vol. 464, pp. 54–58, Apr. 2017, doi: 10.1016/j.jcrysgro.2016.11.096.

[22] G. Dutta, N. Dasgupta, and A. Dasgupta, "Low-temperature ICP-CVD SiN_x as gate dielectric for GaN-based MIS-HEMTs," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 4693–4701, Dec. 2016, doi: 10.1109/TED.2016.2618421.

[23] H. Jiang, C. Liu, Y. Chen, X. Lu, C. W. Tang, and K. M. Lau, "Investigation of *in situ* SiN as gate dielectric and surface passivation for GaN MISHEMTs," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 832–839, Mar. 2017, doi: 10.1109/TED.2016.2638855.

[24] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. New York, NY, USA: Wiley, 2005, pp. 347–350, doi: 10.1063/1.2810086.

[25] N. Komatsu, K. Masumoto, H. Aoki, C. Kimura, and T. Sugino, "Characterization of Si-added aluminum oxide (AlSiO) films for power devices," *Appl. Surf. Sci.*, vol. 256, no. 6, pp. 1803–1806, Jan. 2010, doi: 10.1016/j.apsusc.2009.10.009.

[26] M. V. Fischetti, D. A. Neumayer, and E. A. Cartier, "Effective electron mobility in Si inversion layers in metal–oxide–semiconductor systems with a high-κ insulator: The role of remote phonon scattering," *J. Appl. Phys.*, vol. 90, no. 9, pp. 4587–4608, Nov. 2001, doi: 10.1063/1.1405826.

[27] B. Wang, Z.-Q. Fang, B. Claflin, D. Look, J. Kouvetakis, and Y. K. Yeo, "Electrical characterization and deep-level transient spectroscopy of $Ge_{0.873}Si_{0.104}Sn_{0.023}$ photodiode grown on Ge platform by ultra-high vacuum chemical vapor deposition," *Thin Solid Films*, vol. 654, pp. 77–84, May 2018, doi: 10.1016/j.tsf.2018.03.071.

[28] R. Degraeve, J. L. Ogier, R. Bellens, P. J. Roussel, G. Groeseneken, and H. E. Maes, "A new model for the field dependence of intrinsic and extrinsic time-dependent dielectric breakdown," *IEEE Trans. Electron Devices*, vol. 45, no. 2, pp. 472–481, Feb. 1998, doi: 10.1109/16.658683.

[29] Y. H. Kim, K. Onishi, C. S. Kang, H.-J. Cho, R. Nieh, S. Gopalan, R. Choi, J. Han, S. Krishnan, and J. C. Lee, "Area dependence of TDDB characteristics for HfO_2 gate dielectrics," *IEEE Electron Device Lett.*, vol. 23, no. 10, pp. 594–596, Oct. 2002, doi: 10.1109/LED.2002.803751.

[30] K. Ito, D. Kikuta, T. Narita, K. Kataoka, N. Isomura, K. Kitazumi, and T. Mori, "Band offset of $Al_{1-x}Si_xO_y$ mixed oxide on GaN evaluated by hard X-ray photoelectron spectroscopy," *Jpn. J. Appl. Phys.*, vol. 56, no. 4S, p. 04CG07, Mar. 2017, doi: 10.7567/JJAP.56.04CG07.

[31] A. Crespo-Yepes, J. Martin-Martinez, A. Rothschild, R. Rodriguez, M. Nafria, and X. Aymerich, "Injected charge to recovery as a parameter to characterize the breakdown reversibility of ultrathin HfSiON gate dielectric," *IEEE Trans. Device Mater. Rel.*, vol. 11, no. 1, pp. 126–130, Mar. 2011, doi: 10.1109/tdmr.2010.2098032.