Channel Engineering of Normally-OFF AlGaN/GaN MOS-HEMTs by Atomic Layer Etching and High-κ Dielectric

Qianlan Hu, Sichao Li, Tiaoyang Li, Xin Wang, Xuefei Li, and Yanqing Wu

Abstract—In this letter, normally-off AlGaN/GaN metal-oxide-semiconductor high-electron-mobility transistors with a threshold voltage of 2.2 V have been achieved by an atomic layer etching technique. Combined with surface passivation by atomic layer deposition of composite HfSiO high-κ gate dielectric, a well-controlled gate-recess process with minimized surface damage results in improved interface properties with a low interface trap density of $2.8 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ and suppressed gate leakage current with a high current on/off ratio over $10^{11}$. A maximum current density of 518 mA/mm with an ON-resistance of 10.1 $\Omega$·mm and a high breakdown voltage of 1456 V at an OFF-state current density of 1 $\mu$A/mm are also achieved. In the meantime, the dynamic $R_{on}$ is only 1.2 times the static $R_{on}$ after OFF-state drain voltage stress of 120 V and 2.6 times after 300-V stress.

Index Terms—GaN MOS-HEMTs, normally-off, gate recess, atomic layer etching, high-κ dielectric.

I. INTRODUCTION

O WING to the superior properties of high electric breakdown field, large saturation velocity and low ON-resistance, wide-bandgap GaN-based high electron mobility transistors (HEMTs) have shown great potential for high-frequency power amplifiers and high-voltage power switching applications [1]–[3]. Conventional GaN-based HEMTs are intrinsically normally-on due to the existence of the polarization-induced two-dimensional electron-gas (2DEG) at the heterostructure interface, also known as depletion mode (D-mode) [4]. In practical applications, normally-off property is highly desired for efficient power switching for simplified circuit design and fail-safe operation [5].

Gate recess is a commonly used method to achieve a positive threshold voltage ($V_{th}$) for enhancement mode (E-mode) operation because of simple fabrication process, such as BCl$_3$/Cl$_2$-based inductively coupled plasma dry etching [6]. O$_2$ plasma oxidation followed by diluted HCl de-oxidation [7] and high-temperature thermal oxidation combined with diluted KOH etching [8]. Recently, an O$_2$-BCl$_3$ atomic layer etching technique with precise thickness control and low surface damage has been developed for AlGaN/GaN HEMTs [9], [10]. Traditional HEMTs with Schottky gate suffer from severe gate leakage, resulting in low forward gate bias swing and poor OFF-state characteristics. Metal-oxide-semiconductor HEMTs (MOS-HEMTs) with a thin epitaxial oxide layer in between gate and AlGaN barrier turn out to be an effective way to suppress gate leakage and passivate the surface in the access regions as well [11]. Various gate dielectrics have been investigated, including SiO$_2$ [12], SiN$_x$ [13], Al$_2$O$_3$ [14], HFO$_2$ [15], La$_2$O$_3$ [16], MgCaO [17] and LaHfO$_x$ [18]. Although the gate leakage current can be suppressed, the interface property between dielectric and barrier remains to be a challenge.

In this work, normally-off AlGaN/GaN MOS-HEMTs with recessed gate were fabricated using O$_2$-BCl$_3$ atomic layer etching to precisely control the gate recess process and minimize surface damage. The resulting devices exhibit a high drive current and a low ON-resistance with threshold voltage ($V_{th}$) over 2 V. Moreover, high-κ gate dielectric HfSiO grown by atomic layer deposition (ALD) is adopted for reduced leakage current, lower interface trap density, and better surface passivation. Extremely low gate leakage down to $10^{-9}$ mA/mm and large breakdown voltage of 1456 V at an OFF-state current density of 1 $\mu$A/mm can be achieved. In the meantime, the dynamic $R_{on}$ is only 1.2 times the static $R_{on}$ after OFF-state $V_{DS}$ stress of 120 V, indicating the suppression of current collapse using the above process.

II. DEVICE FABRICATION

Fig. 1 (a) depicts the schematic cross-section of the fabricated normally-off AlGaN/GaN MOS-HEMT on silicon (111) substrate. The epitaxial layer consists of a 4-$\mu$m C-doped GaN buffer, a 300-nm undoped GaN channel, a 1-nm AlN interlayer, and a 20-nm Al$_{0.25}$Ga$_{0.75}$N barrier. Device isolation was carried out using multi-energy ion implantation followed by plasma enhanced atomic layer deposition of a 60-nm AlN etching mask. Gate recess was performed using O$_2$-BCl$_3$ hybrid etching for atomic layer thickness control.
In this case, the AlGaN barrier was recessed by means of repeated cycles of oxidation and etching using inductively coupled plasma, and each cycle consisted of forming a thin oxide layer on the top and etching away by low power BCl$_3$ etching. The etching rate was precisely controlled at 1.5 nm/cycle. Due to the lower volatility of AlCl$_x$ relative to GaCl$_x$, and smaller bond energy of Ga-N compared to Al-N, the recess etching stopped at the AlN interlayer [19]. This resembles a self-limiting process since BCl$_3$ etches the oxidized layer much faster than unoxidized regions [20]. Fig. 1 (c) shows atomic force microscopy image of the trench profile of the gate recessed area with a width of 2 μm, and the surface roughness in the gate window is shown in Fig. 1 (d) with a root mean square roughness of 0.27 nm, confirming the high uniformity of the recess etching. The source-drain ohmic contacts were formed by Ti/Al/Ni/Au multilayer metal deposition followed by rapid thermal annealing (RTA) at 870 °C for 30 s in N$_2$. A 15-nm HfSiO high-$\kappa$ dielectric was deposited at 300 °C with Tetrakis(dimethylamino)hafnium, Tris(dimethylamino)silane and ozone as precursors. Finally, Ni/Au metal stack was deposited as gate electrodes followed by pads window opening. The MOS-HEMTs have a gate length of 1 μm, a gate-source spacing of 3.5 μm, a gate-drain distance of 21 μm, and a gate width of 100 μm unless otherwise noted. The contact resistance was extracted to be 0.6 Ω·mm from transfer-length-method (TLM) model.

III. Results and Discussion

The 2DEG density induced by the piezoelectric polarization between AlGaN and GaN depends on the thickness of AlGaN, and as the etching thickness increases, the density decreases which leads to a positive shift of $V_{th}$ as shown in Fig. 2 (a). E-mode operation can be achieved with negligible hysteresis (38 mV at 1 KHz) and frequency dispersion as shown in capacitance-voltage (CV) characteristics in Fig. 2 (b). Multi-frequency conductance method was employed to map the interface properties and the equivalent parallel conductance $G_p/\omega$ as a function of radial frequency ($\omega$) is given by the equation: $G_p/\omega = q\omega \tau_{it} D_{it}/[1+(\omega \tau_{it})^2]$, where $q$ is the electron charge and $\tau_{it}$ is the time constant. The trap state density $D_{it}$ can be extracted using equation: $D_{it} = 2.5 (G_p/\omega)_{peak}/q$ [21]. $D_{it}$ as a function of energy level (EC-ET) is shown in Fig. 2 (d) and the trap state density is in the range of $2.8 \times 10^{11} - 3.6 \times 10^{12}$ eV$^{-1}$cm$^{-2}$ for energy span of 0.24-0.31 eV below the GaN conduction band, exhibiting a high quality of the interface owing to the low-damage recess and excellent interface quality. Fig. 3 (a) compares the transfer characteristics of GaN MOS-HEMTs where $V_{th}$ values are extracted to be $-4.8$ V and 2.2 V for D-mode and E-mode devices by linear extrapolation, respectively. The peak conductance $G_m$ increases from 148 mS/mm to 170 mS/mm after recess, suggesting an efficient gate electro-static control using the high-$\kappa$ gate dielectric. FATFET ($I_G = 100$ μm, $W_G = 100$ μm) mobility of 520 cm$^2$/V·s was extracted [22]. In the transfer characteristics at $V_{DS} = 5$ V shown in Fig. 3 (b), as small subthreshold slope (SS) of 104 mV/dec and high on/off current ratio over $10^{11}$ can be achieved. The $I_D$ to $I_G$ ratio is more than $10^6$ even at a large forward bias of 6 V, suggesting minimal leakage current of the high-$\kappa$ dielectric. Comparison of output characteristics for the MOS-HEMTs with and without gate
have a LGD of 16 different quiescent drain bias points. Both D-mode and E-mode devices current recess is shown in Fig. 3 (c), where the maximum output current $I_{D,\text{MAX}}$ of 519 mA/mm at $V_G = 6$ V is achieved for the E-mode device, comparable to 512 mA/mm at $V_G = -1$ V for the D-mode device. A low ON-resistance ($R_{on}$) of 10.1 $\Omega \cdot$ mm is also obtained for the E-mode device, slightly larger than 9.2 $\Omega \cdot$ mm of D-mode device. It is worth noting that the drain current of the D-mode device drops significantly at high drain bias, indicating a self-heating induced by high current density and a charge trapping induced by high electric field between drain and gate [23].

Pulsed $I_D$–$V_D$ measurement under fast switching with different quiescent bias points were carried out to evaluate the current collapse characteristics as shown in Fig. 4 (a), where the pulsed output characteristics of the E-mode MOS-HEMT are plotted together at quiescent bias points from ($V_{GS}$, $V_{DS}$) = (0 V, 10 V) to (0 V, 300 V) at $V_G = 5$ V. The inset shows the pulsed-IV measurement setup where the pulsed output characteristics of the E-mode MOS-HEMT shows the great potential of the optimized channel engineering of AlGaN/GaN MOS-HEMTs for power switching applications.

Fig. 4. (a) Pulsed-IV output characteristics of E-mode MOS-HEMT under quiescent points from ($V_{GS}$, $V_{DS}$) = (0 V,10 V) to (0 V,300 V) at $V_G = 5$ V. The inset is the measurement setup. (b) The ratio of dynamic on-resistance of the fabricated D/E-mode MOS-HEMTs at different quiescent drain bias points. Both D-mode and E-mode devices have a $L_{GD}$ of 16 $\mu$m.

IV. Conclusion

Normally-off AlGaN/GaN MOS-HEMTs have been fabricated using a precisely controlled and low-damage atomic layer etching technique. The device exhibits a threshold voltage of 2.2 V and a saturation current of 518 mA/mm with a low ON-resistance of 10.1 $\Omega \cdot$ mm. In combination with the high-k gate dielectric grown by atomic layer deposition, the gate leakage current and interface trap density have been suppressed simultaneously, leading to a high on/off ratio of 10$^2$ and enhanced breakdown voltage of 1456 V. Pulsed-IV measurement is performed with satisfactory dynamic characteristics attributed to low trap state density. These results show the great potential of the optimized channel engineering of AlGaN/GaN MOS-HEMTs for power switching applications.

REFERENCES


