Channel Engineering of Normally-OFF AlGaN/GaN MOS-HEMTs by Atomic Layer Etching and High-κ Dielectric

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***Abstract*— In this letter, normally-OFF AlGaN/GaN metal–oxide–semiconductor high-electron-mobility transistors with a threshold voltage of 2.2 V have been achieved by an atomic layer etching technique. Combined with surface passivation by atomic layer deposition of composite HfSiO high-κ gate dielectric, a well-controlled gate-recess process with minimized surface damage results in improved interface properties with a low interface trap density of 2.8 × 10^{11} $eV^{-1}cm^{-2}$ and suppressed gate leakage current with a high current on/off ratio over 10^{11}. A maximum current density of 518 mA/mm with an ON-resistance of 10.1 Ω · mm and a high breakdown voltage of 1456 V at an OFF-state current density of 1 μA/mm are also achieved. In the meantime, the dynamic R_{on} is only 1.2 times the static R_{on} after OFF-state drain voltage stress of 120 V and 2.6 times after 300-V stress.**

***Index Terms*— GaN MOS-HEMTs, normally-off, gate recess, atomic layer etching, high-κ dielectric.**

I. Introduction

OWING to the superior properties of high electric breakdown field, large saturation velocity and low ON-resistance, wide-bandgap GaN-based high electron mobility transistors (HEMTs) have shown great potential for high-frequency power amplifiers and high-voltage power switching applications [1]–[3]. Conventional GaN-based HEMTs are intrinsically normally-on due to the existence of the polarization-induced two-dimensional electron-gas (2DEG) at the heterostructure interface, also known as depletion mode (D-mode) [4]. In practical applications, normally-off property is highly desired for efficient power switching for simplified circuit design and fail-safe operation [5].

Gate recess is a commonly used method to achieve a positive threshold voltage (V_{th}) for enhancement mode (E-mode) operation because of simple fabrication process, such as BCl_3/Cl_2-based inductively coupled plasma dry etching [6], O_2 plasma oxidation followed by diluted HCl de-oxidation [7] and high-temperature thermal oxidation combined with diluted KOH etching [8]. Recently, an O_2-BCl_3 atomic layer etching technique with precise thickness control and low surface damage has been developed for AlGaN/GaN HEMTs [9], [10]. Traditional HEMTs with Schottky gate suffer from severe gate leakage, resulting in low forward gate bias swing and poor OFF-state characteristics. Metal-oxide-semiconductor HEMTs (MOS-HEMTs) with a thin epitaxial oxide layer in between gate and AlGaN barrier turn out to be an effective way to suppress gate leakage and passivate the surface in the access regions as well [11]. Various gate dielectrics have been investigated, including SiO_2 [12], SiN_x [13], Al_2O_3 [14], HfO_2 [15], La_2O_3 [16], MgCaO [17] and $LaHfO_x$ [18]. Although the gate leakage current can be suppressed, the interface property between dielectric and barrier remains to be a challenge.

In this work, normally-off AlGaN/GaN MOS-HEMTs with recessed gate were fabricated using O_2-BCl_3 atomic layer etching to precisely control the gate recess process and minimize surface damage. The resulting devices exhibit a high drive current and a low ON-resistance with threshold voltage (V_{th}) over 2 V. Moreover, high-κ gate dielectric HfSiO grown by atomic layer deposition (ALD) is adopted for reduced leakage current, lower interface trap density, and better surface passivation. Extremely low gate leakage down to 10^{-9} mA/mm and large breakdown voltage of 1456 V at an OFF-state current density of 1 μA/mm can be achieved. In the meantime, the dynamic R_{on} is only 1.2 times the static R_{on} after OFF-state V_{DS} stress of 120 V, indicating the suppression of current collapse using the above process.

II. Device Fabrication

Fig. 1 (a) depicts the schematic cross-section of the fabricated normally-off AlGaN/GaN MOS-HEMT on silicon (111) substrate. The epitaxial layer consists of a 4-μm C-doped GaN buffer, a 300-nm undoped GaN channel, a 1-nm AlN interlayer, and a 20-nm $Al_{0.25}Ga_{0.75}N$ barrier. Device isolation was carried out using multi-energy ion implantation followed by plasma enhanced atomic layer deposition of a 60-nm AlN etching mask. Gate recess was performed using O_2-BCl_3 hybrid etching for atomic layer thickness control.

Manuscript received June 26, 2018; revised July 12, 2018; accepted July 14, 2018. Date of publication July 18, 2018; date of current version August 23, 2018. This work was supported by the Key Basic Research Program of Hubei Province under Grant 2017AAA127. The review of this letter was arranged by Editor G. H. Jessen. *(Corresponding author: Yanqing Wu.)*

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Digital Object Identifier 10.1109/LED.2018.2856934

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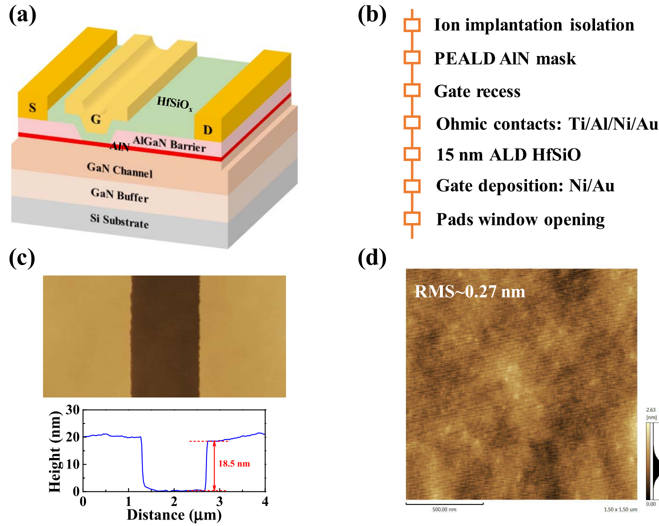

Fig. 1. (a) Cross section schematic view of the GaN MOS-HEMT. (b) Fabrication of recessed gate devices. (c) Trench profile of the 1 μm width recessed gate window. (d) 1.5 μm × 1.5 μm surface morphology of the channel area.

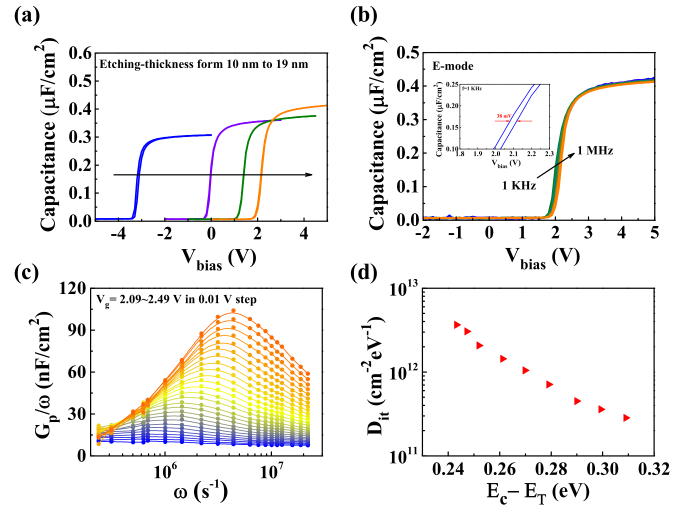

Fig. 2. (a) Capacitance-voltage (CV) characteristics with etching thickness from 10-19 nm. (b) Multi-frequency CV characteristics of E-mode device under double sweep. (c) Experimental and fitting curves of G_p/ω vs. ω, where the G_p/ω is equivalent parallel conductance and ω is radial frequency. (d) Trap state density as a function of energy level.

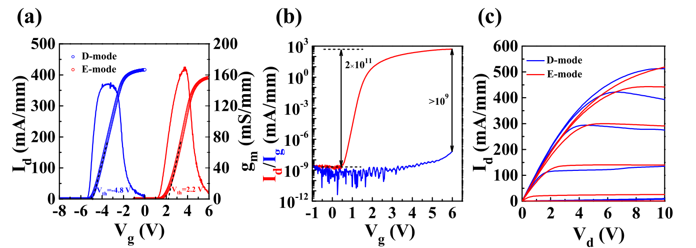

Fig. 3. (a) Comparison of transfer characteristics for D/E-mode MOS-HEMTs in linear scale. (b) Transfer characteristic and gate leakage current of E-mode device in semi-log scale. (c) Comparison of output characteristics for D/E-mode MOS-HEMTs.

In this case, the AlGaN barrier was recessed by means of repeated cycles of oxidation and etching using inductively coupled plasma, and each cycle consisted of forming a thin oxide layer on the top and etching away by low power BCl_3 etching. The etching rate was precisely controlled at 1.5 nm/cycle. Due to the lower volatility of $AlCl_x$ relative to $GaCl_x$, and smaller bond energy of Ga-N compared to Al-N, the recess etching stopped at the AlN interlayer [19]. This resembles a self-limiting process since BCl_3 etches the oxidized layer much faster than unoxidized regions [20]. Fig. 1 (c) shows atomic force microscopy image of the trench profile of the gate recessed area with a width of 2 μm, and the surface roughness in the gate window is shown in Fig. 1 (d) with a root mean square roughness of 0.27 nm, confirming the high uniformity of the recess etching. The source-drain ohmic contacts were formed by Ti/Al/Ni/Au multilayer metal deposition followed by rapid thermal annealing (RTA) at 870 °C for 30 s in N_2. A 15-nm HfSiO high-κ dielectric was deposited at 300 °C with Tetrakis(dimethylamino)hafnium, Tris(dimethylamino)silane and ozone as precursors. Finally, Ni/Au metal stack was deposited as gate electrodes followed by pads window opening. The MOS-HEMTs have a gate length of 1 μm, a gate-source spacing of 3.5 μm, a gate-drain distance of 21 μm, and a gate width of 100 μm unless otherwise noted. The contact resistance was extracted to be 0.6 $\Omega \cdot$ mm from transfer-length-method (TLM) model.

III. Results and Discussion

The 2DEG density induced by the piezoelectric polarization between AlGaN and GaN depends on the thickness of AlGaN, and as the etching thickness increases, the density decreases which leads to a positive shift of V_{th} as shown in Fig. 2 (a). E-mode operation can be achieved with negligible hysteresis (38 mV at 1 KHz) and frequency dispersion as shown in capacitance-voltage (CV) characteristics in Fig. 2 (b). Multi-frequency conductance method was employed to map the interface properties and the equivalent parallel conductance G_p/ω as a function of radial frequency (ω) is given by the equation: $G_p/\omega = q\omega\tau_{it}D_{it}/[1+(\omega\tau_{it})^2]$, where q is the electron charge and τ_{it} is the time constant. The trap state density D_{it} can be extracted using equation: $D_{it} = 2.5(G_p/\omega)_{peak}/q$ [21]. D_{it} as a function of energy level (E_C-E_T) is shown in Fig. 2 (d) and the trap state density is in the range of 2.8×10^{11}-3.6×10^{12} $eV^{-1}cm^{-2}$ for energy span of 0.24-0.31 eV below the GaN conduction band, exhibiting a high quality of the interface owing to the low-damage recess and excellent interface quality.

Fig. 3 (a) compares the transfer characteristics of GaN MOS-HEMTs where V_{th} values are extracted to be −4.8 V and 2.2 V for D-mode and E-mode devices by linear extrapolation, respectively. The peak conductance G_m increases from 148 mS/mm to 170 mS/mm after recess, suggesting an efficient gate electro-static control using the high-κ gate dielectric. FATFET (L_G = 100 μm, W_G = 100 μm) mobility of 520 $cm^2/V \cdot s$ was extracted [22]. In the transfer characteristics at V_{DS} = 5 V shown in Fig. 3 (b), a small subthreshold slope (SS) of 104 mV/dec and high on/off current ratio over 10^{11} can be achieved. The I_D to I_G ratio is more than 10^9 even at a large forward bias of 6 V, suggesting minimal leakage current of the high-κ dielectric. Comparison of output characteristics for the MOS-HEMTs with and without gate

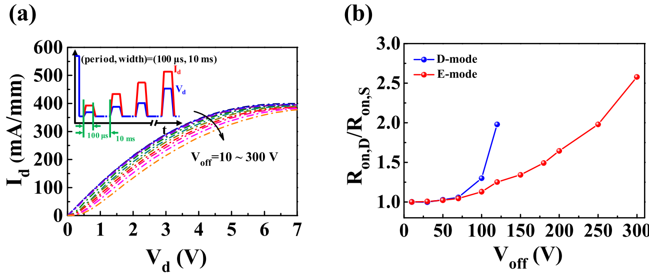

Fig. 4. (a) Pulsed-IV output characteristics of E-mode MOS-HEMT under quiescent points from (V_{GS}, V_{DS}) = (0 V,10 V) to (0 V,300 V) at V_G = 5 V. The inset is the measurement setup. (b) The ratio of dynamic ON-resistance of the fabricated D/E-mode MOS-HEMTs at different quiescent drain bias points. Both D-mode and E-mode devices have a L_{GD} of 16 μm.

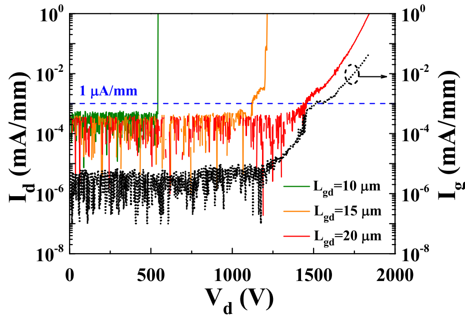

Fig. 5. OFF-state breakdown characteristics of the E-mode devices with gate-drain distance of 10, 15 and 20 μm at V_G = 0 V. Gate and source electrodes are biased at 0 V.

recess is shown in Fig. 3 (c), where the maximum output current $I_{D,MAX}$ of 519 mA/mm at $V_G = 6$ V is achieved for the E-mode device, comparable to 512 mA/mm at $V_G = -1$ V for the D-mode device. A low ON-resistance (R_{on}) of 10.1 $\Omega \cdot$ mm is also obtained for the E-mode device, slightly larger than 9.2 $\Omega \cdot$ mm of D-mode device. It is worth noting that the drain current of the D-mode device drops significantly at high drain bias, indicating a self-heating induced by high current density and a charge trapping induced by high electric field between drain and gate [23].

Pulsed I_D–V_D measurement under fast switching with different quiescent bias points were carried out to evaluate the current collapse characteristics as shown in Fig. 4 (a), where the pulsed output characteristics of the E-mode MOS-HEMT are plotted together at quiescent bias points from (V_{GS}, V_{DS}) = (0 V, 10 V) to (0 V, 300 V) at V_G = 5 V. The inset shows the pulsed-IV measurement setup where the measurement pulse width is 50 μs (total width 100 μs) with a period of 10 ms. The E-mode device exhibits an increase of 250 % in the dynamic R_{on} after high drain bias stress of 300 V, indicating the current collapse induced by charge trapping has been effectively suppressed [24]. The ratio of dynamic ON-resistance of the fabricated D/E-mode MOS-HEMTs are extracted and plotted in Fig. 4 (b), where the D-mode device suffers from more severe current collapse which can be attributed to the higher field between drain and gate with more electron injection to traps in the access region.

Fig. 5 shows the OFF-state breakdown characteristics of the E-mode devices with varying gate-drain distance. It can be seen that the gate leakage is about two orders lower than I_D, suggesting that the leakage current is mainly originated from the source injection current at a drain bias up to 1200 V when the OFF-state gate leakage has been effectively suppressed by the HfSiO high-κ dielectric. The leakage from both source and gate increases when V_D further increases beyond 1200 V and eventually leads to hard breakdown. The breakdown voltage increases with gate-drain distance due to the length-dependent electric field. The highest breakdown voltage reaches to 1456 V at an OFF-state current density of 1 μA/mm at L_{GD} = 21 μm, resulting in a lateral breakdown strength of 0.91 MV/cm and a power figure of merit ($BV^2/R_{on,sp}$) of 733 MW/cm^2.

IV. Conclusion

Normally-off AlGaN/GaN MOS-HEMTs have been fabricated using a precisely controlled and low-damage atomic layer etching technique. The device exhibits a threshold voltage of 2.2 V and a saturation current of 518 mA/mm with a low ON-resistance of 10.1 $\Omega \cdot$ mm. In combination with the HfSiO high-κ gate dielectric grown by atomic layer deposition, the gate leakage current and interface trap density have been suppressed simultaneously, leading to a high on/off ratio of 10^{11} and enhanced breakdown voltage of 1456 V. Pulsed-IV measurement is performed with satisfactory dynamic characteristics attributed to low trap state density. These results show the great potential of the optimized channel engineering of AlGaN/GaN MOS-HEMTs for power switching applications.

References

[1] N. Ikeda *et al.*, "GaN power transistors on Si substrates for switching applications," *Proc. IEEE*, vol. 98, no. 7, pp. 1151–1161, Jul. 2010, doi: 10.1109/JPROC.2009.2034397.

[2] J. Das, J. Everts, J. Van Den Keybus, M. V. Hove, D. Visalli, P. Srivastava, D. Marcon, K. Cheng, M. Leys, and S. Decoutere, "A 96% efficient high-frequency DC–DC converter using E-mode GaN DHFETs on Si|," *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1370–1372, Oct. 2011, doi: 10.1109/LED.2011.2162393.

[3] M. Ishida, T. Ueda, T. Tanaka, and D. Ueda, "GaN on Si technologies for power switching devices," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3053–3059, Oct. 2013, doi: 10.1109/TED.2013.2268577.

[4] M. Wang, Y. Wang, C. Zhang, B. Xie, C. Wen, J. Wang, Y. Hao, W. Wu, K. J. Chen, and B. Shen, "900 V/1.6 m$\Omega \cdot$cm^2 normally OFF Al_2O_3/GaN MOSFET on silicon substrate," *IEEE Trans. Electron Devices*, vol. 61, no. 6, pp. 2035–2040, Jun. 2014, doi: 10.1109/TED.2014.2315994.

[5] T. Oka and T. Nozawa, "AlGaN/GaN recessed MIS-gate HFET with high-threshold-voltage normally-off operation for power electronics applications," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 668–670, Jul. 2008, doi: 10.1109/LED.2008.2000607.

[6] K.-W. Kim, S.-D. Jung, D.-S. Kim, H.-S. Kang, K.-S. Im, J.-J. Oh, J.-B. Ha, J.-K. Shin, and J.-H. Lee, "Effects of TMAH treatment on device performance of normally off Al_2O_3/GaN MOSFET," *IEEE Electron Device Lett.*, vol. 32, no. 7, pp. 1376–1378, Oct. 2011, doi: 10.1109/LED.2011.2163293.

[7] Q. Zhou, L. Liu, A. Zhang, B. Chen, Y. Jin, Y. Shi, Z. Wang, W. Chen, and B. Zhang, "7.6 V threshold voltage high-performance normally-off Al_2O_3/GaN MOSFET achieved by interface charge engineering," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 165–168, Feb. 2016, doi: 10.1109/LED.2015.2511026.

[8] S. Lin *et al.*, "A GaN HEMT structure allowing self-terminated, plasma-free etching for high-uniformity, high-mobility enhancement-mode devices," *IEEE Electron Device Lett.*, vol. 37, no. 4, pp. 377–380, Apr. 2016, doi: 10.1109/LED.2016.2533422.

[9] S. D. Burnham, K. Boutros, P. Hashimoto, C. Butler, D. W. S. Wong, M. Hu, and M. Micovic, “Gate-recessed normally-off GaN-on- Si HEMT using a new O_2-BCl_3 digital etching technique,” *Physica Status Solidi*, vol. 7, no. 7, pp. 2010–2012, Jun. 2010, doi: 10.1002/pssc.200983644.

[10] D. Marcon, M. Van Hove, B. De Jaeger, N. Posthuma, D. Wellekens, S. You, X. Kang, T.-L. Wu, M. Willems, S. Stoffels, and S. Decoutere, “Direct comparison of GaN-based E-mode architectures (recessed MISHEMT and p-GaN HEMTs) processed on 200 mm GaN-on-Si with Au-free technology,” *Proc. SPIE*, vol. 9363, p. 936311, Mar. 2015, doi: 10.1117/12.2077806.

[11] P. D. Ye, B. Yang, K. K. Ng, J. Bude, G. D. Wilk, S. Halder, and J. C. M. Hwang, “GaN metal-oxide-semiconductor high-electron-mobility-transistor with atomic layer deposited Al_2O_3 as gate dielectric,” *Appl. Phys. Lett.*, vol. 86, no. 6, pp. 063501-1–063501-3, Jan. 2005, doi: 10.1063/1.1861122.

[12] F. Husna, M. Lachab, M. Sultana, V. Adivarahan, Q. Fareed, and A. Khan, “High-temperature performance of AlGaN/GaN MOSHEMT with SiO2 gate insulator fabricated on Si (111) substrate,” *IEEE Trans. Electron Devices*, vol. 59, no. 9, pp. 2424–2429, Sep. 2012, doi: 10.1109/TED.2012.2204888.

[13] M. Hua, Z. Zhang, J. Wei, J. Lei, G. Tang, K. Fu, Y. Cai, B. Zhang, and K. J. Chen, “Integration of LPCVD-SiN_x gate dielectric with recessed-gate E-mode GaN MIS-FETs: Toward high performance, high stability and long TDDB lifetime,” in *IEDM Tech. Dig.*, Dec. 2017, pp. 10.4.1–10.4.4, doi: 10.1109/IEDM.2016.7838388.

[14] S. Huang, Q. Jiang, K. Wei, and G. Liu, “High-temperature low-damage gate recess technique and ozone-assisted ALD-grown Al_2O_3 gate dielectric for high-performance normally-off GaN MIS-HEMTs,” in *IEDM Tech. Dig.*, Dec. 2014, pp. 17.4.1–17.4.4, doi: 10.1109/IEDM.2014.7047071.

[15] X. Sun, O. I. Saadat, K. S. Chang-Liao, T. Palacios, S. Cui, and T. P. Ma, “Study of gate oxide traps in HfO_2/AlGaN/GaN metal-oxide-semiconductor high-electron-mobility transistors by use of ac transconductance method,” *Appl. Phys. Lett.*, vol. 102, no. 10, pp. 103504, Mar. 2013, doi: 10.1063/1.4795717.

[16] H.-C. Chiu, C.-W. Lin, C.-H. Chen, C.-W. Yang, C.-K. Lin, J.-S. Fu, L.-B. Chang, R.-M. Lin, and K.-P. Hsueh, “Low hysteresis dispersion La_2O_3 AlGaN/GaN MOS-HEMTs,” *J. Electrochem. Soc.*, vol. 157, no. 2, pp. H160–H164, 2010, doi: 10.1149/1.3264622.

[17] H. Zhou, X. Lou, N. J. Conrad, M. Si, H. Wu, S. Alghamdi, S. Guo, R. G. Gordon, and P. D. Ye, “High-performance InAlN/GaN MOSHEMTs enabled by atomic layer epitaxy MgCaO as gate dielectric,” *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 556–559, May 2016, doi: 10.1109/LED.2016.2537198.

[18] Y. C. Lin, Y. X. Huang, G. N. Huang, C. H. Wu, J. N. Yao, C. M. Chu, S. Chang, C. C. Hsu, H. L. Jin, and K. Kakushima, “Enhancement-mode GaN MIS-HEMTs with $LaHfO_x$ gate insulator for power application,” *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1101–1104, Aug. 2017, doi: 10.1109/LED.2017.2722002.

[19] S. A. Smith, C. A. Wolden, M. D. Bremser, A. D. Hanser, R. F. Davis, and W. V. Lampert, “High rate and selective etching of GaN, AlGaN, and AlN using an inductively coupled plasma,” *Appl. Phys. Lett.*, vol. 71, no. 25, pp. 3631–3633, Oct. 1997, doi: 10.1063/1.120463.

[20] H. Hahn, G. Lükens, N. Ketteniss, H. Kalisch, and A. Vescan, “Recessed-gate enhancement-mode AlGaN/GaN heterostructure field-effect transistors on Si with record DC performance,” *Appl. Phys. Exp.*, vol. 4, no. 11, p. 114102, 2011, doi: 10.1143/APEX.4.114102.

[21] S. Liu, S. Yang, Z. Tang, Q. Jiang, C. Liu, M. Wang, B. Shen, and K. J. Chen, “Interface/border trap characterization of Al_2O_3/AlN/GaN metal-oxide-semiconductor structures with an AlN interfacial layer,” *Appl. Phys. Lett.*, vol. 106, no. 5, pp. 295–298, Feb. 2015, doi: 10.1063/1.4907861.

[22] M. Tao, S. Liu, B. Xie, C. P. Wen, J. Wang, Y. Hao, W. Wu, K. Cheng, B. Shen, and M. Wang, “Characterization of 880 V normally off GaN MOSHEMT on silicon substrate fabricated with a plasma-free, self-terminated gate recess process,” *IEEE Trans. Electron Devices*, vol. 65, no. 4, pp. 1453–1457, Apr. 2018, doi: 10.1109/TED.2018.2808345.

[23] Z. Tang, S. Huang, X. Tang, B. Li, and K. J. Chen, “Influence of AlN passivation on dynamic ON-resistance and electric field distribution in high-voltage AlGaN/GaN-on-Si HEMTs,” *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2785–2792, Aug. 2014, doi: 10.1109/TED.2014.2333063.

[24] S. Yang, Y. Lu, H. Wang, S. Liu, C. Liu, and K. J. Chen, “Dynamic gate stress-induced VTH shift and its impact on dynamic RON in GaN MIS-HEMTs,” *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 157–160, Feb. 2016, doi: 10.1109/LED.2015.2505334.